Pre-test and Post-test Translation

The tests were in Norwegian. The following is a translation of the questions. To avoid presenting identical questions twice (which would have been the result with one section for the pre-test and another for the post-test) pre-test only questions are marked with “PRE” and the corresponding post-test only questions with “POST”.

Part A: Busses (multiple choice, only one alternative to be checked)

1-PRE) Which of these lines is NOT part of a bus?
[ ] Address line
[ ] Control line
[ ] Return line
[ ] Data line

1-POST) Which is NOT a good argument for having hierarchical busses in a computer?
[ ] Wanting to separate slow from quick units
[ ] A long bus has higher transmission delay
[ ] More busses means more units can transmit data at the same time
[ ] With some units specialized busses may be an advantage
[ ] The locality principle makes it less likely that remote units will be used

2) A multiplexed bus
[ ] demands fewer lines than a dedicated bus
[ ] gives better performance than a dedicated bus
[ ] cannot be used outside the computer
[ ] makes arbitration more complicated than a dedicated bus
[ ] cannot be used with modern RAM technology

3-PRE) What type of arbitration implies that one specific unit always selects the bus master?
[ ] Distributed arbitration
[ ] Dynamic arbitration
[ ] Centralised arbitration
[ ] Static arbitration
[ ] Structured arbitration

3-POST) Which statement is INCORRECT?
[ ] Arbitration is unnecessary for a synchronous bus
[ ] A bus is a shared transmission medium
[ ] A bus is the most usual connection structure in a computer
[ ] A bus typically contains control, address, and data lines
[ ] Arbitration is not necessary if only one of the units attached to the bus may be the bus master

4) Which is true about the communication over a bus?
[ ] Several units may communicate simultaneously if they are adjacent on the bus
[ ] One unit can always send to another as long as the other is not sending
[ ] The bus goes only one way
[ ] Only one unit may send on the bus at a time

5-PRE) Which is INCORRECT about a multiplexed bus?
[ ] A multiplexed bus has fewer lines than a non-multiplexed bus
[ ] A multiplexed bus is a hierarchy of busses
[ ] A multiplexed bus demands more complicated circuits
[ ] A multiplexed bus cannot send data and address simultaneously
[ ] A multiplexed bus has lower performance than a non-multiplexed one

5-POST) Which is correct about arbitration?
[ ] During arbitration, the signals to be sent are coded
[ ] During arbitration, it is decided which unit will be allowed to use the bus
[ ] Arbitration verifies that all lines in the bus are working
[ ] Arbitration is caused by the delay in the bus transmission
[ ] Arbitration is used to increase the performance of the bus

6) A given bus between three or more units contains 16 data lines and 16 address lines. These may be used to
[ ] make 2^{16} different connections, each able to transmit 16 bits
[ ] Transmit 16 bits in each direction between two units
[ ] Simultaneously transmit 16 bits between two units
[ ] make 4 connections between various units, simultaneously transmitting 1 byte at each connection
[ ] transmit a multiple of 16 bits between two units. How many bits the bus can handle depends on its length

Part B: Addressing modes

Given a computer with a number of registers R0, R1, R2, …, and data memory. Initial values for the memory, registers and some variables are shown in the figure below.

Main mem.

value	addr
233	7
15	8
4	9
15	10
17	11
12	12
17	13
9	14
7	15
8	16
21	17
19	18
7	19
9	20

Registers

reg	value
R0	0
R1	1
R2	4
R3	3
R4	15

Variables

Name	addr
VAR1	16
VAR2	8
VAR3	10
TABLE	11

1) What is the value of R1 after performing MOV R1, 17?

2-PRE) What is the value of R1 after performing MOV R1, [R4]?
2-POST) What is the value of R1 after performing MOV R1, #9?

3-PRE) What is the value of R1 after performing MOV R1, TABLE(R3)?
3-POST) What is the value of R1 after performing MOV R1, 8(R2)?

4) What is the value of R1 after performing MOV R1, R3?

5-PRE) What is the value of R1 after performing MOV R1, 4(R3)?
5-POST) What is the value of R1 after performing MOV R1, [14]?

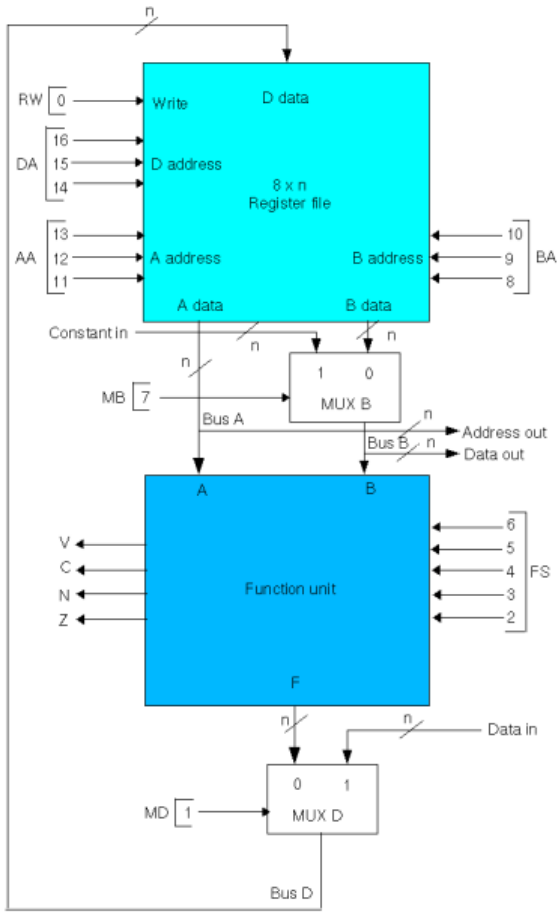
Part C: Control words

Given the control unit schema and the control word codes and format illustrated in the above figures, please answer the following questions:

1-PRE) What is the control word for `R7 ← ~R5`
where x implies unused bits?

1-POST) What is the control word for `R7 ← R1 + ~R5 +1`
where x implies unused bits?

2) What is the control word for `R7 ← R2 XOR R0`
where x implies unused bits?



DA, AA, BA		MB		FS		MD		RW	
Function	Code	Function	Code	Function	Code	Function	Code	Function	Code
R0	000	Register	0	*F* = A	00000	Function	0	No Write	0
R1	001	Constant	1	*F* = A + 1	00001	Data In	1	Write	1
R2	010			*F* = A + B	00010				
R3	011			*F* = A + B + 1	00011				
R4	100			*F* = A + ~B	00100				
R5	101			*F* = A+ ~B+ 1	00101				
R6	110			*F* = A - 1	00110				
R7	111			*F* = ~A	00111				
				F = A ^ B	01000				
				F = A v B	01010				
				F = A XOR B	01100				
				F = A	01110				
				F = sr A	10000				
				F = sl A	10001