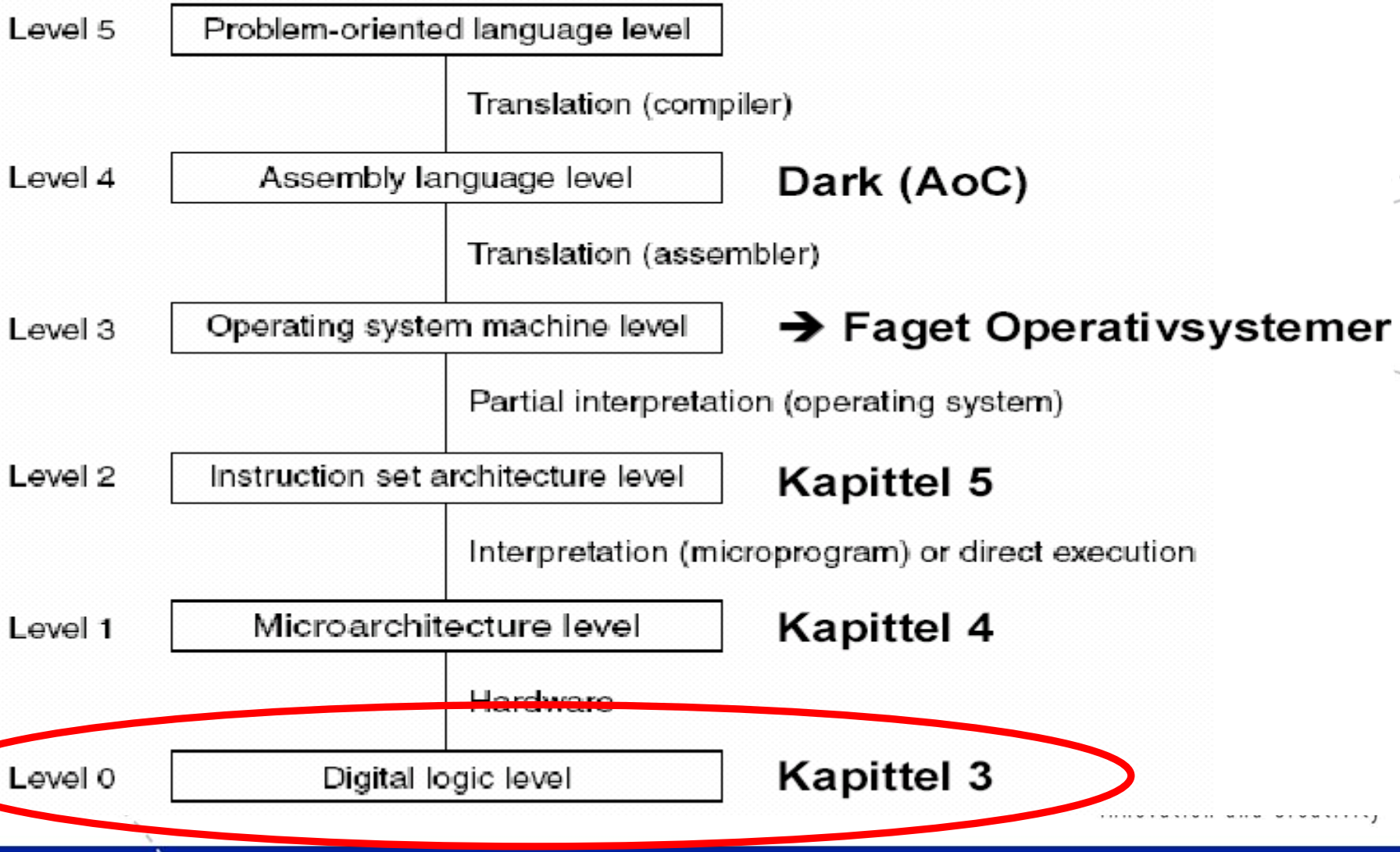
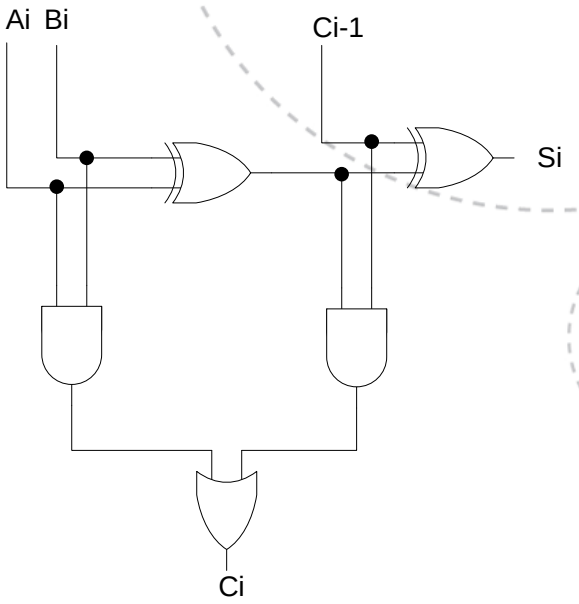
Digital logic level: Oppsummering

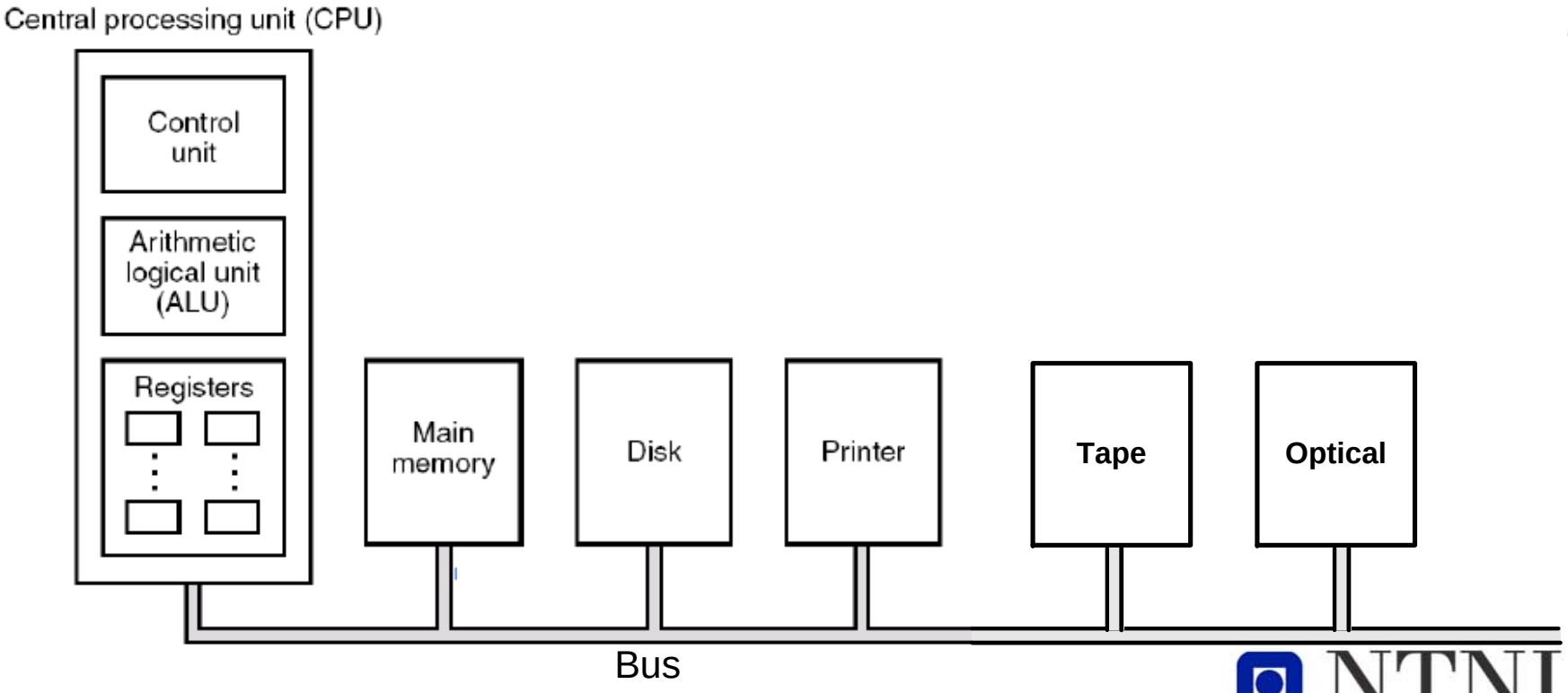


Nivå 0: Digtalekretsar

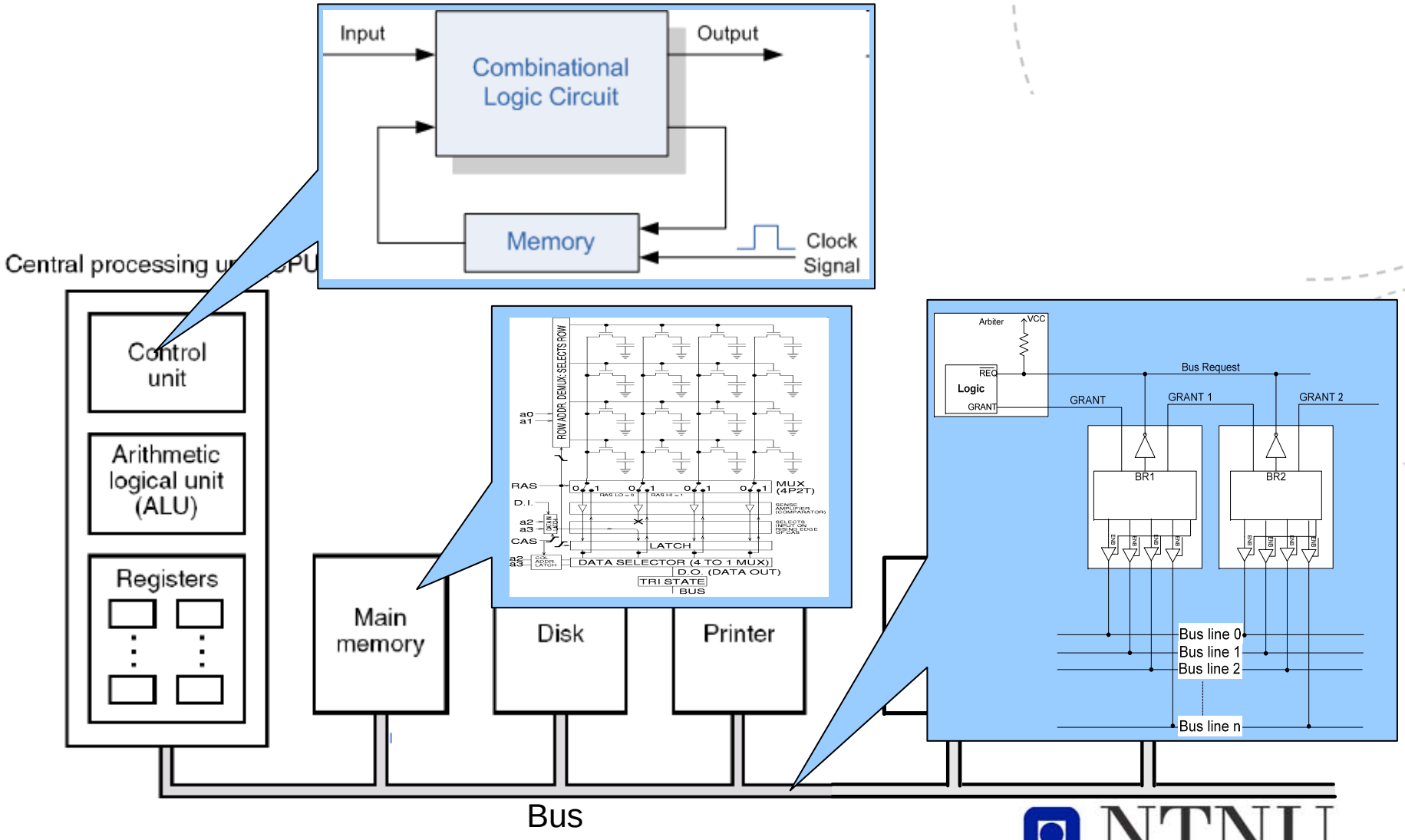
- Fundamentale komponentar
  - AND, OR, NOT,NAND, NOR XOR porter
  - D-vipper for lagring av ett bit
- Samansette komponentar
  - Aritmetiske kretsar –
    - adderere, skiftere, …
  - Dekodere
  - Multiplekser
  - Registre
    - 8, 16, 32, 64 vipper



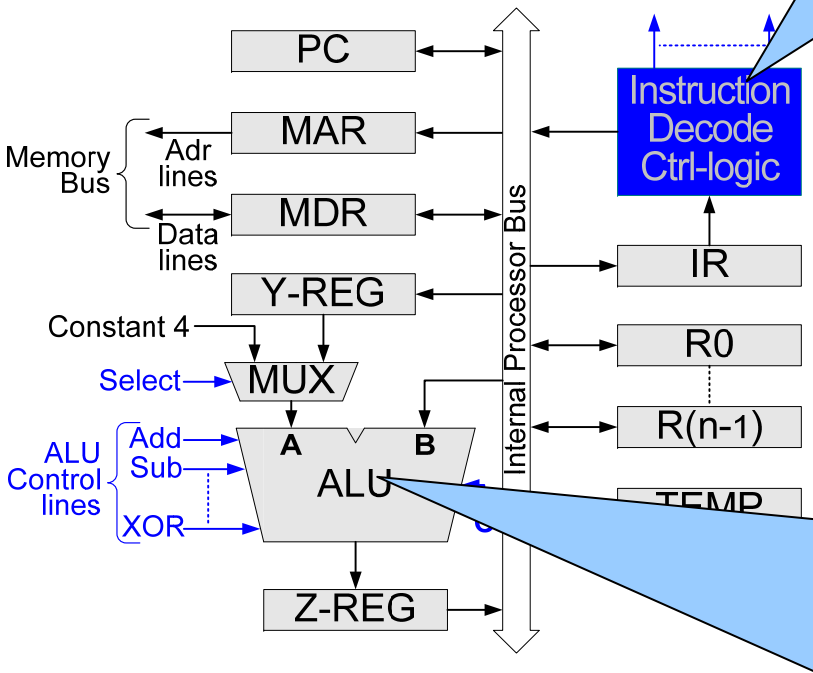
Kva er inni dingsar ”under paseret”



Kva er inni dingsar ”under panseret”

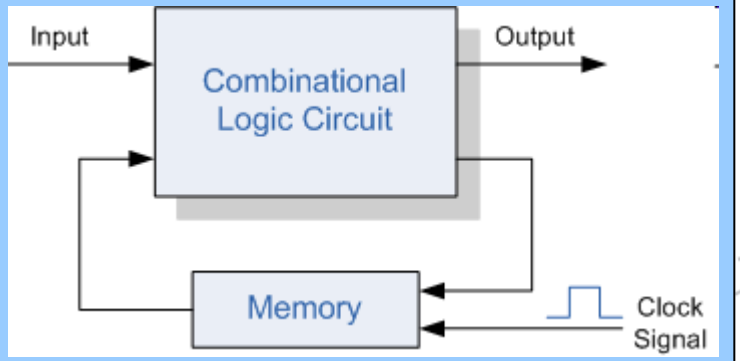


Digital logic level



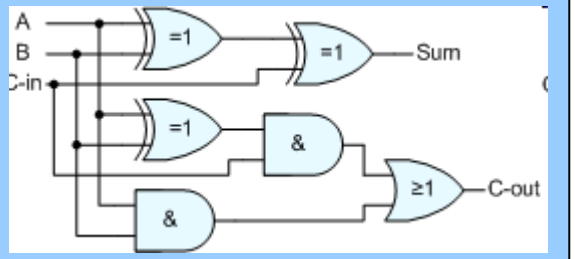
Sekvensiellekretsar

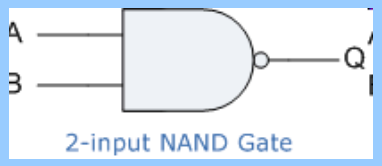
Minne

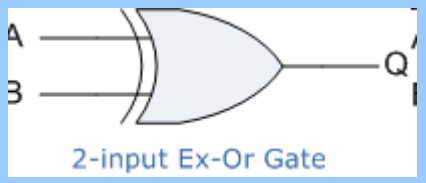


kombinatoriske kretsar

Logic functions





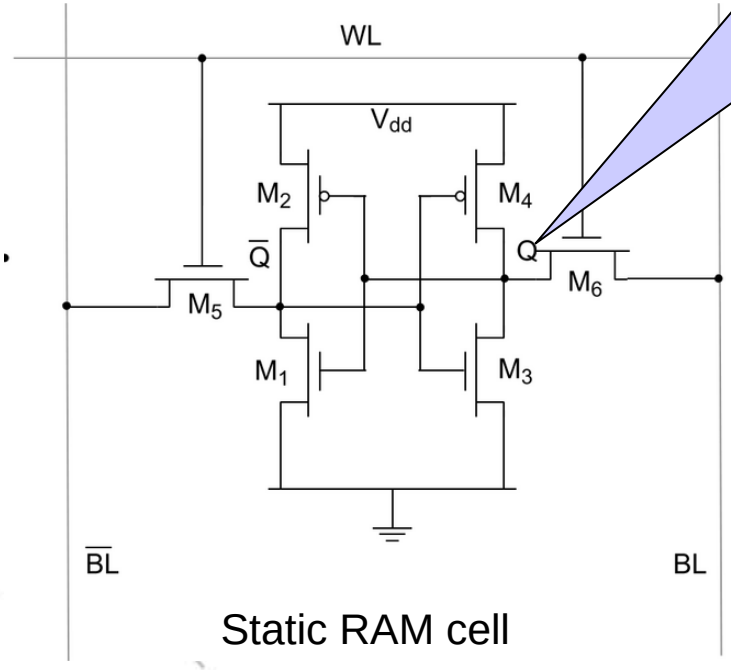


Random Access Memory (RAM)

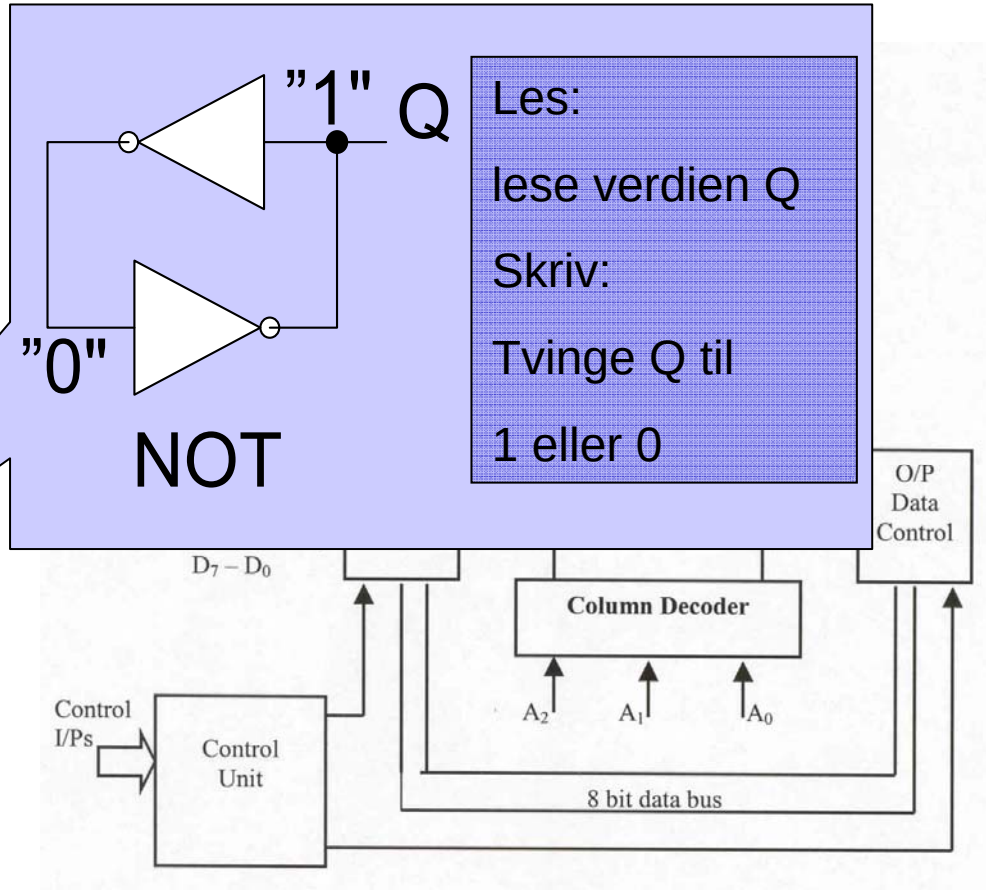
- Data kan aksesseres i tilfeldig rekkefølge
  - Direct Access Memory – harddisker
  - Serial Access Memory - bånd
- Krever strøm for å bevare innhold
- Statisk RAM
  - Matrise med D-flip-flop (= det vi har sett til nå)
  - 6 transistorer pr. bit
  - Dyrt, stort og raskt
- Dynamisk RAM
  - 1 transistor og 1 kondensator pr. bit
  - Billig, lite og ”tregt”
  - Krever oppfrisking

RAM: statisk og dynamisk

- Statisk
  - Rask
  - Stor minnecelle (areal)
  - Stort effektforbruk
  - Må ikkje oppfriskast
  - Enkelt grensesnitt

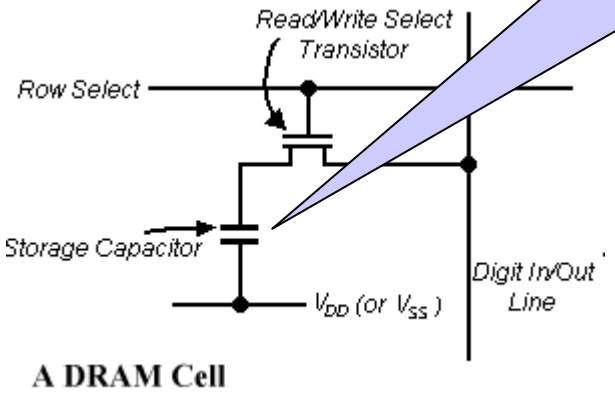


Static RAM cell

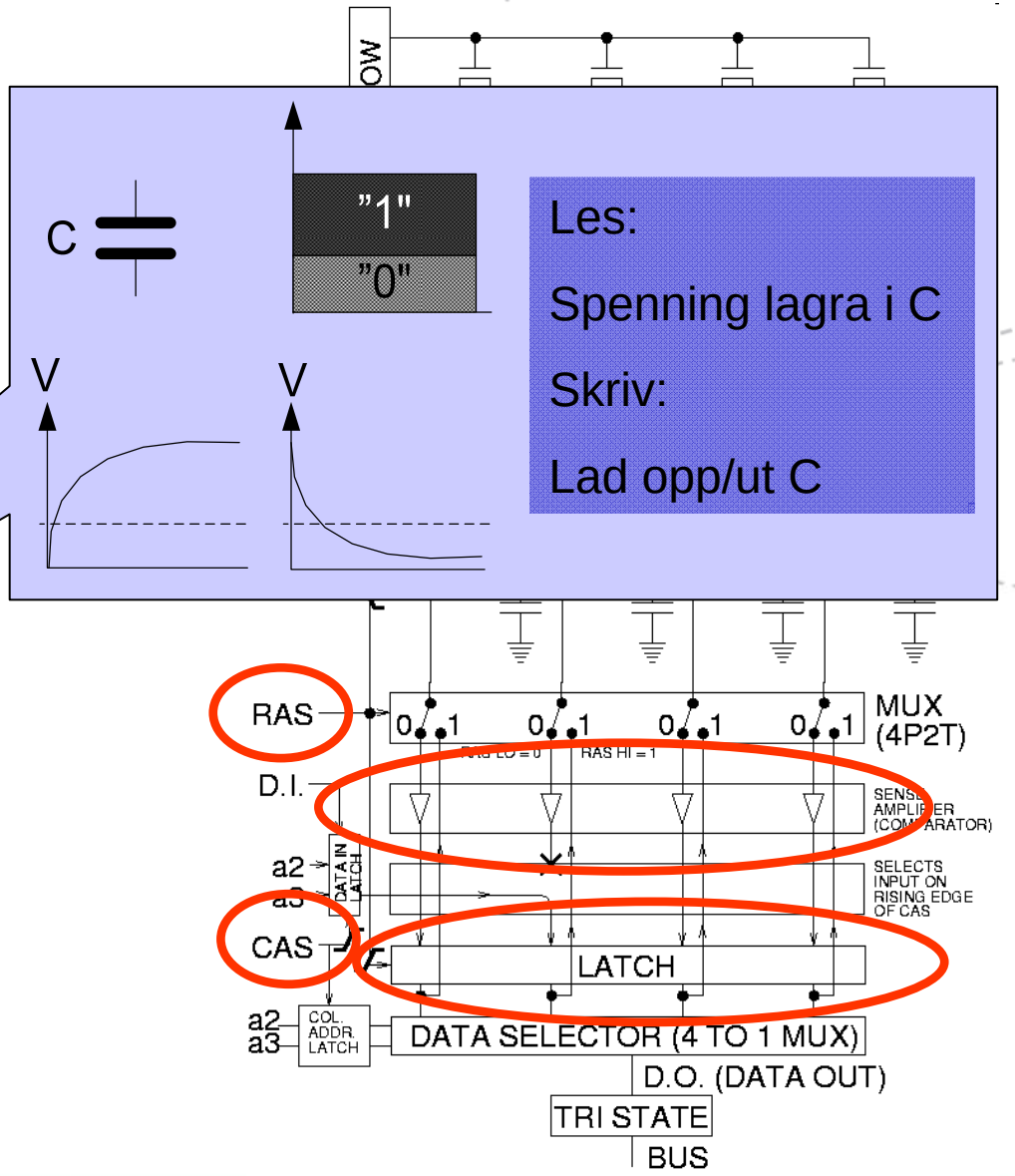


RAM: statisk og dynamisk

- Dynamisk
  - Ikkje så rask
  - Liten minnecelle (areal)
  - Lite effektforbruk
  - Må ha oppfrisking
  - Meir komplisert grensesnitt (DRAM-kontroller)



A DRAM Cell



Andre minnetypar: nonVolatile ROM

- ROM (Read Only Memory)
  - Lagre program eller data som aldri skal endrast
  - Fast innhald definert ved produksjon
  - Celle brukar lite areal, bit kopla til ”1” (VCC) eller ”0” (GND)
  - Cella i seg sjølv brukar ikkje strøm ekstremt lite effektforbruk
  - Stort sett kunn for masseproduksjon (ved mange billigast)
  - Ofte grensesnitt som statisk RAM, men utan skriving
- PROM (Programmable Read Only Memory)
  - Som ROM, men kan programmerast minst ein gong
  - Innehalde kan definerast etter produksjon
  - Mange typar
    - PROM: programmerast ein gong
    - EPROM (Erasable) kan slettast
    - EEPROM (Electrically) kan slettast elektrisk
    - Ofte lang programmerings tid
- Flash memory
    - ”EEPROM med rask programmering”
    - Billig
    - Programmerast i blokker
    - Kan endrast ca 1000 000 gonger

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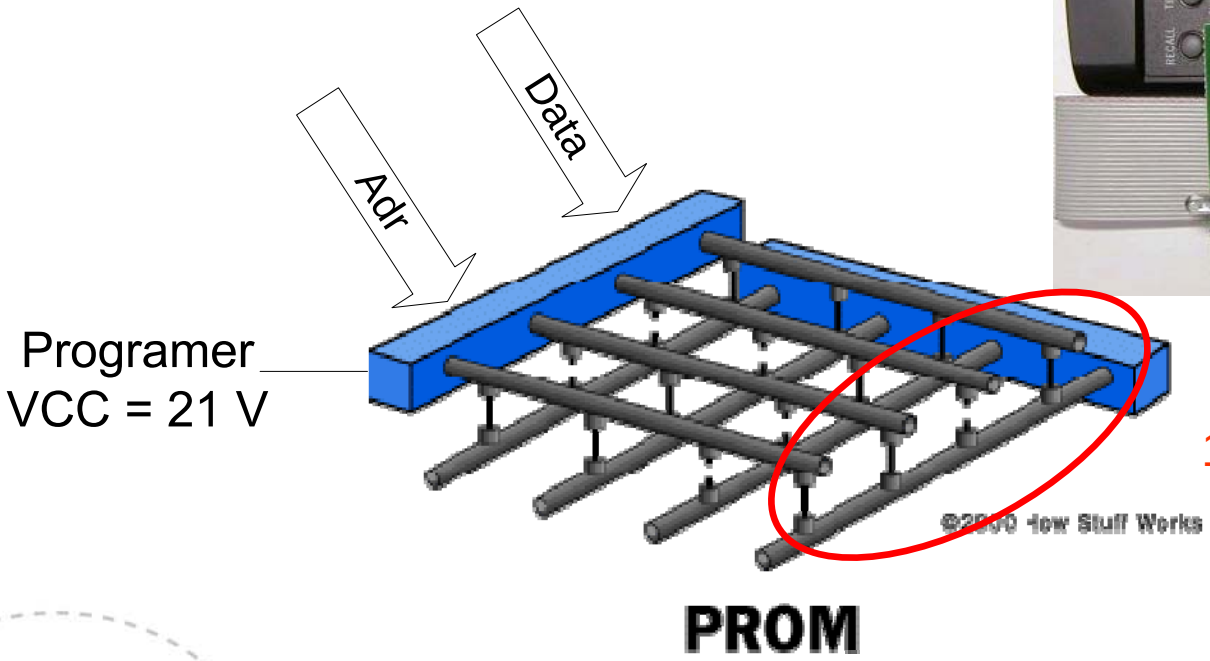
PROM, EPROM, EEPROM

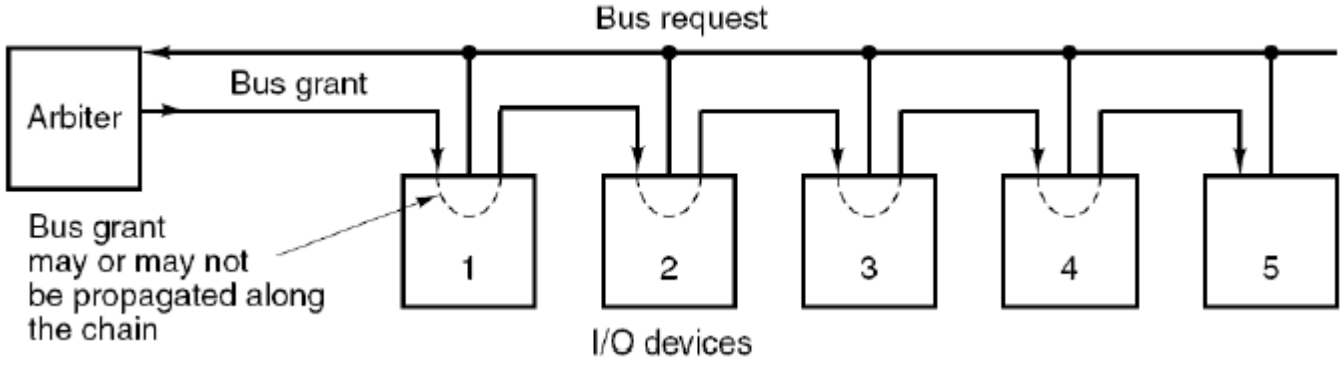
- PROM (Programmable Read Only Memory)
  - Programmerast ofte ved å ”brenne” innterne sikringar i brikken
  - Ofte brukt i mikrokontrollerar (8051)
    - Brukaren kan då lage eit program som lastast ned
    - Fint i masse produksjon
    - Lastar ned program i produksjonslinja



Bussar

- Tilgong til buss (Three state buffer)
- Synkron / Asynkron
- Serielle bussar
- Parallelle bussar
- Arbitrering: Kven kontrollerar bussen

Arbitrering: Kven kontrollerar bussen



- Eksempel: eining **2** og **3** vill ha buss
  - Buss er ledig
  - 2 og 3 legg ut ”Bus request”
  - Arbiter mottar ”Bus request”
  - Arbiter legg ut ”Bus grant”
  - 1 mottar ”Bus grant”, 1 har **ikkje** lagt ut ”Bus request”, **sender** ”Bus grant vidare”
  - 2 mottar ”Bus grant”, 2 har lagt ut ”Bus request”, sender **ikkje** ”Bus grant vidare”
  - 2 er no buss ”master” og kan bruke bussen
  - 3 mottar **ikkje** ”Bus grant”, fortsetter å legje ut ”Bus request”
  - 2 ferdig med buss
  - 1 deretter 2 sender ”Bus grant” vidare
  - 3 mottar ”Bus grant”, sender **ikkje** ”Bus grant vidare”
  - 3 er no buss ”master” og kan bruke bussen

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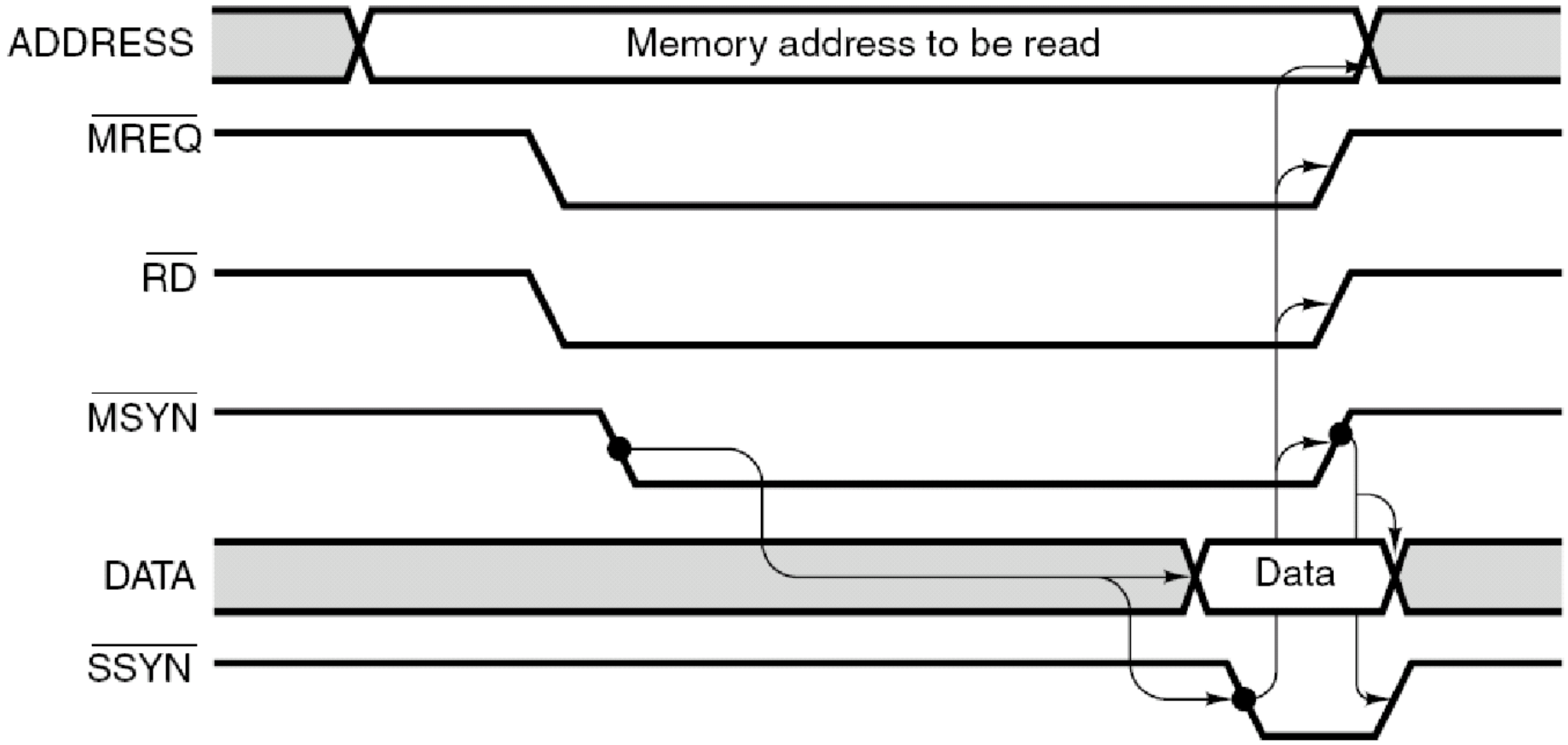
Bussoverføring: adresse, data, kontroll



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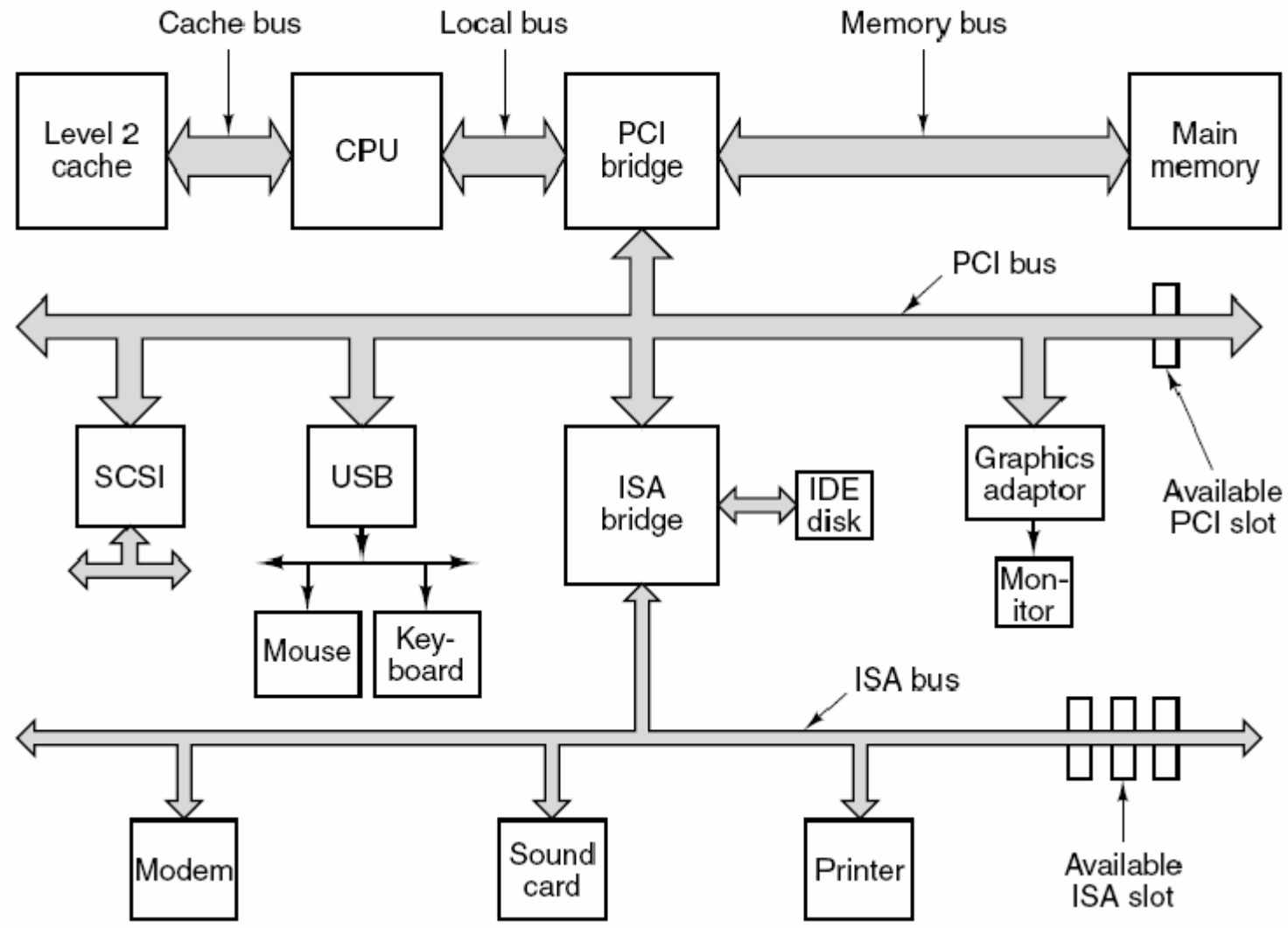
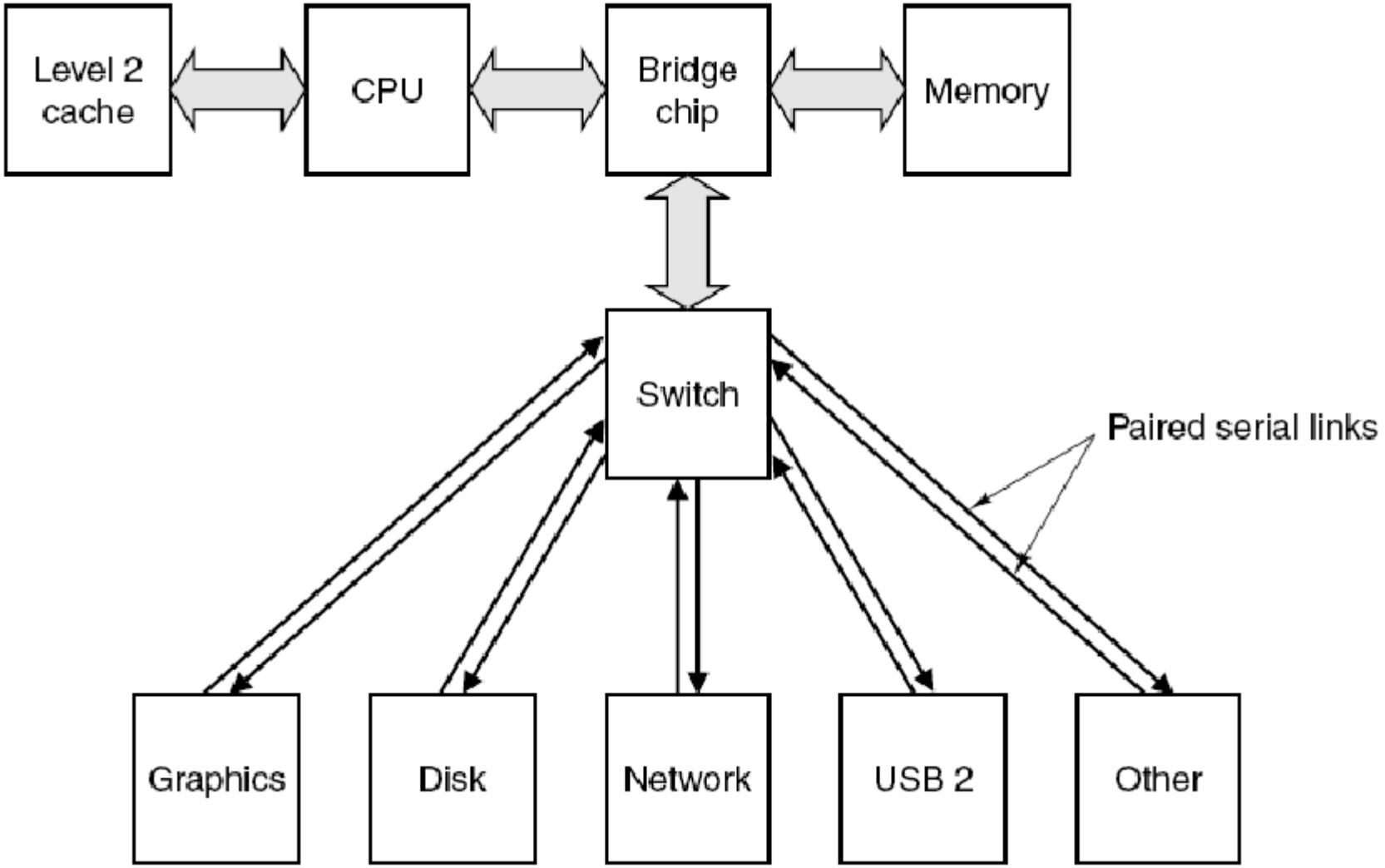
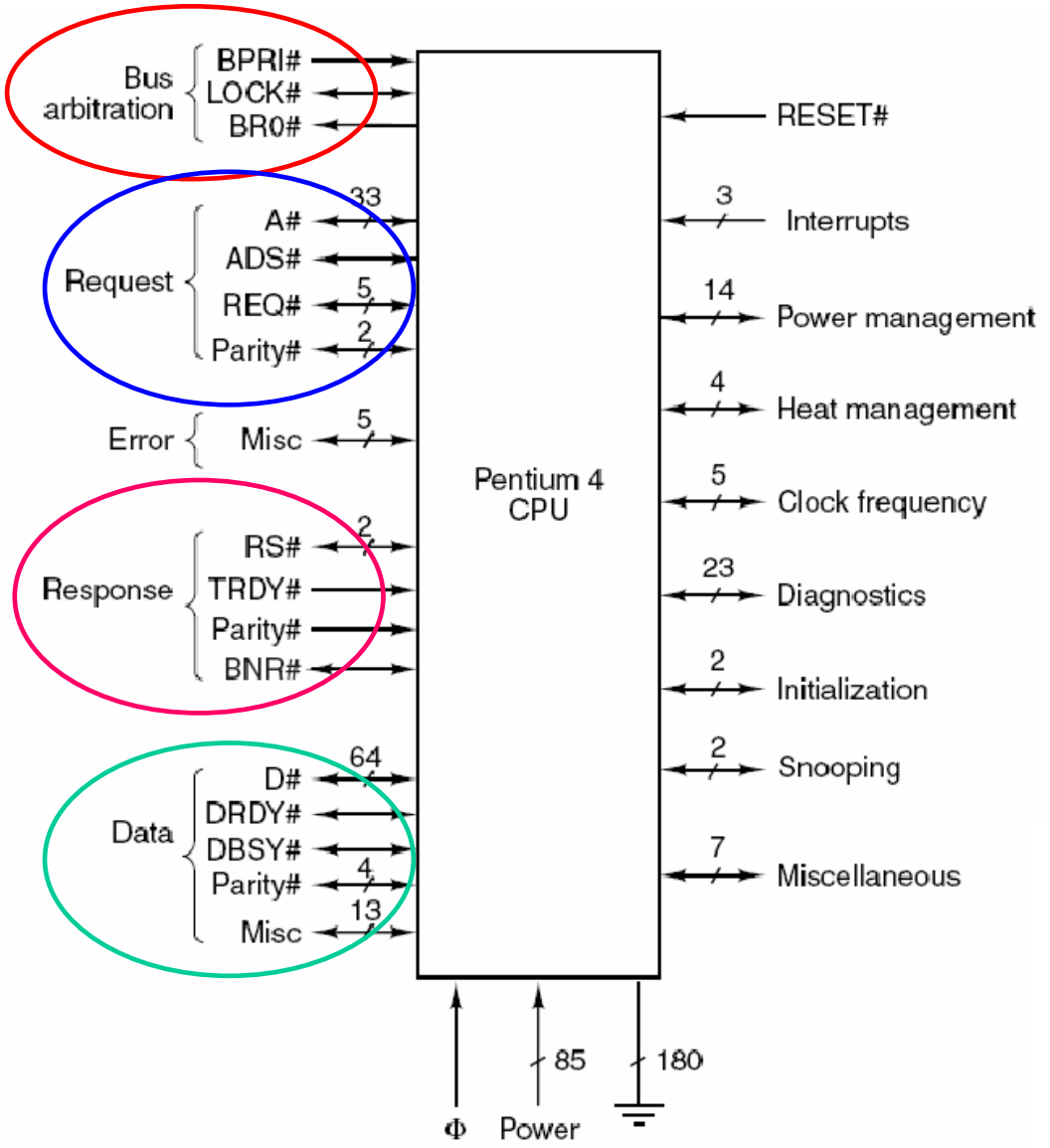
Tidlig Pentium-system



PCI Express punkt-til-punkt



P4 Logisk utsjåande



BR0: Bus request

BPRI: Høgprioritet bus request

LOCK: Eigarskap av buss

A: Adresse linjer 33 ((36) 3 alltid 0)

ADS: Adresse gyldig

REQ: Bus cycle (read, write word, block osv)

Parity: Paritet for ”A” og ”REQ”

RS: Respons Status kode

TRDY: Slave klar

Parity: Paritet for gruppa

BNR: Wait state

D: Datalinjer

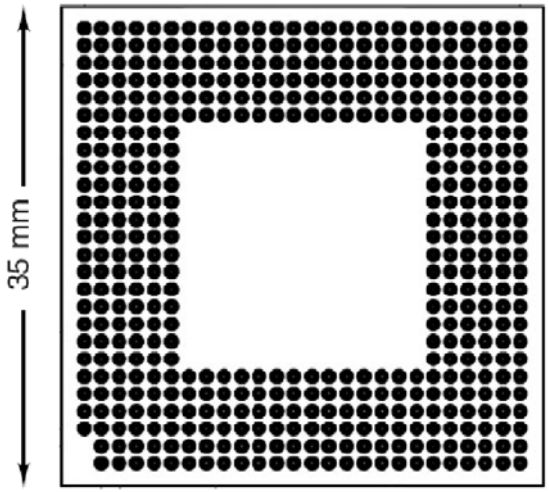
DRDY: Data gyldig

DBSY: Buss ibruk

Parity: Paritet for data

P4 fysisk utsjåande

- Mange pakkar 423 pinnar, 478 pinnar, 775 pinnar osv
  - 85 VCC (for 478)
  - 180 GND (for 478)



- Strenge krav til utlegg
  - Stømforsyning
  - Klokkelinjer
  - Avkobling
  - Signallinjer

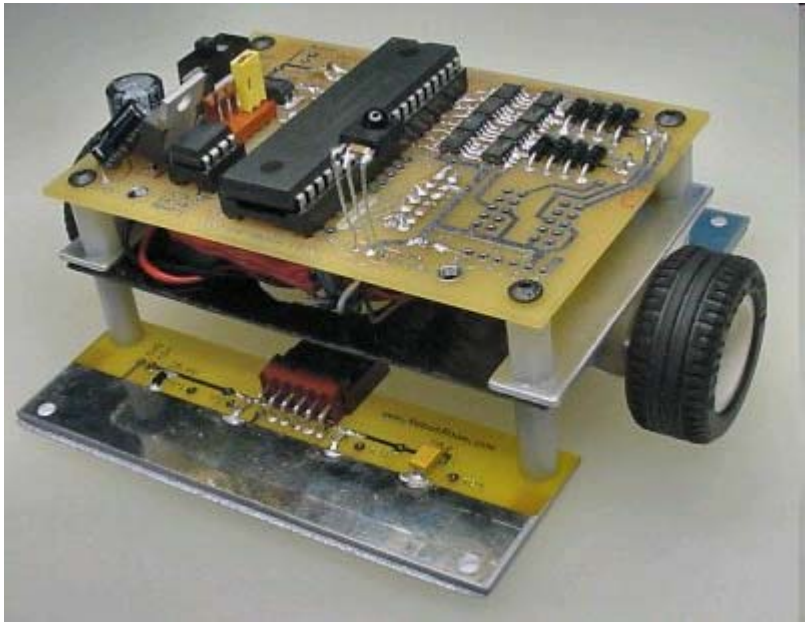
- Strenge krav til kjøling
  - Effektforbruk opp mot 200W

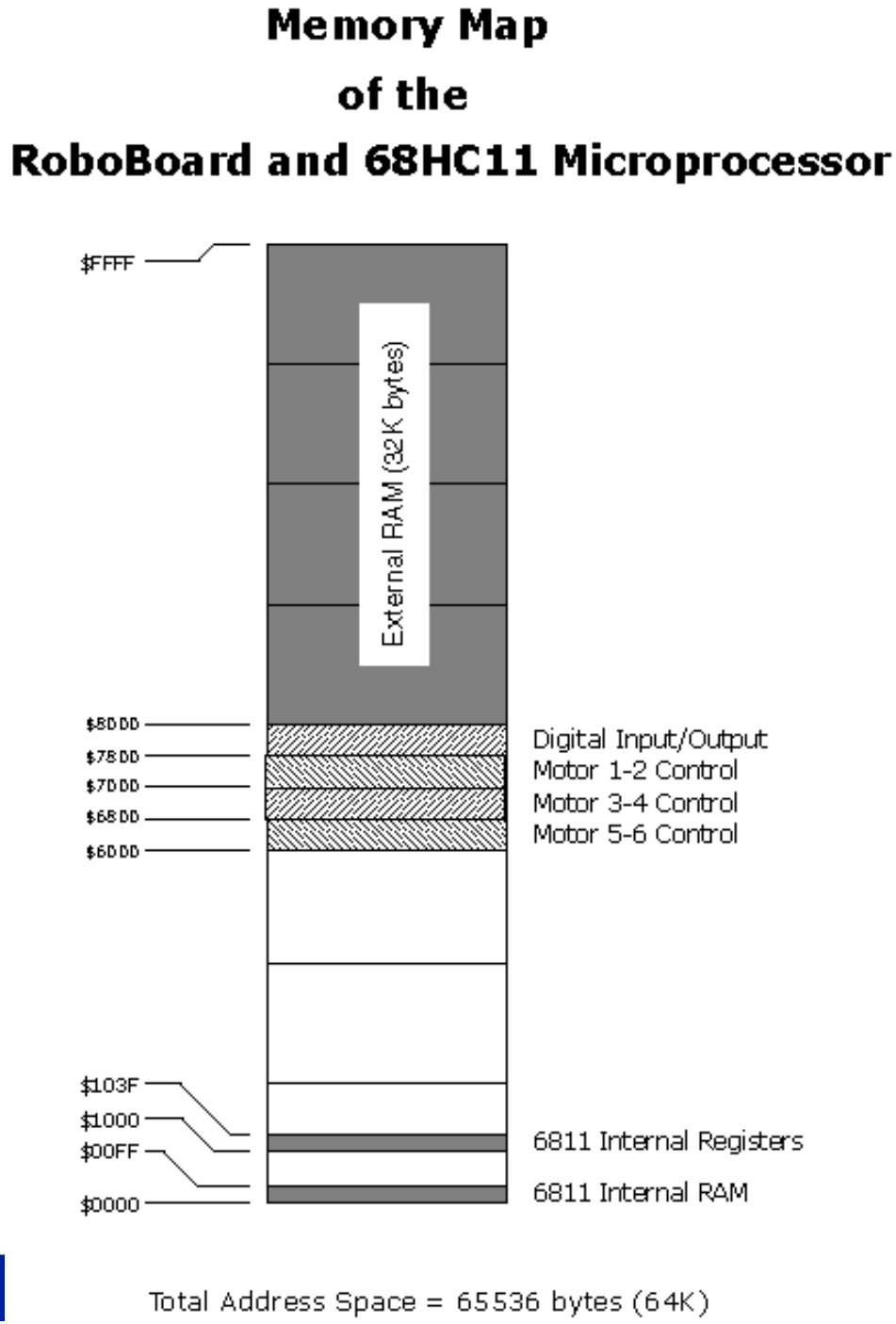
Adresse dekoding

- Kan adressere einheitar
  - Minne
  - I/O
  - Register
- Adresse dekoding
  - Eining må kunne adresserast (veljast)
  - Må ha eit minnekart for systemet
    - Kva ligg på kva minne adresse
    - For eksempel, prosessor kan då aksesera einheitar ved å lese/skrive til minne adresser
    - Som programmerarar brukar me minnekarte til å finne kva adresse me skal bruke for å lese/skrive til ein eining
    - Som maskinvarekonstruktørar må me lage eit minnekart for systemet

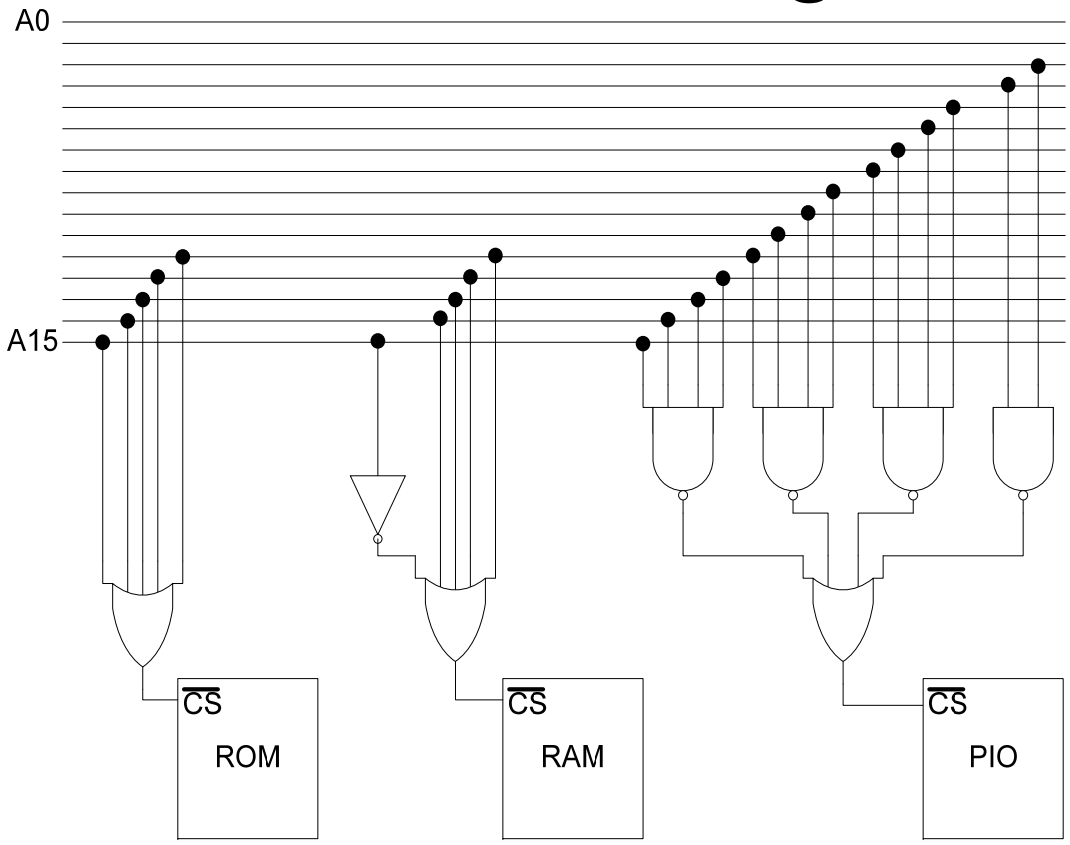
Adresse dekoding

- Minnekart
  - Kva ligg på kva minne adresse
  - Kan då aksesere einheitar ved å lese/skrive til minne adresser





Adresse dekoding finne adr. område



ROM:

Dekod: 0000 0XXX XXXX XXXX

Høg: 0000 0111 1111 1111

0 7 F F

Låg: 0000 0000 0000 0000

0 0 0 0

RAM:

Dekod: 1000 0XXX XXXX XXXX

Høg: 8 7 F F

Låg: 8 0 0 0

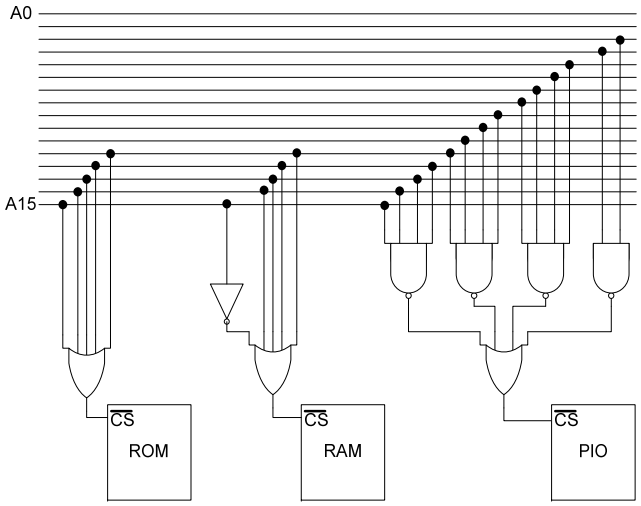
PIO:

Dekod: 1111 1111 1111 11XX

Høg: F F F F

Låg: F F F C

Adresse dekoding lage adr. kart



PIO:

Dekod: 1111 1111 1111 11XX

Høg: F F F F

Låg: F F F C

RAM:

Dekod: 1000 0XXX XXXX XXXX

Høg: 8 7 F F

Låg: 8 0 0 0

ROM:

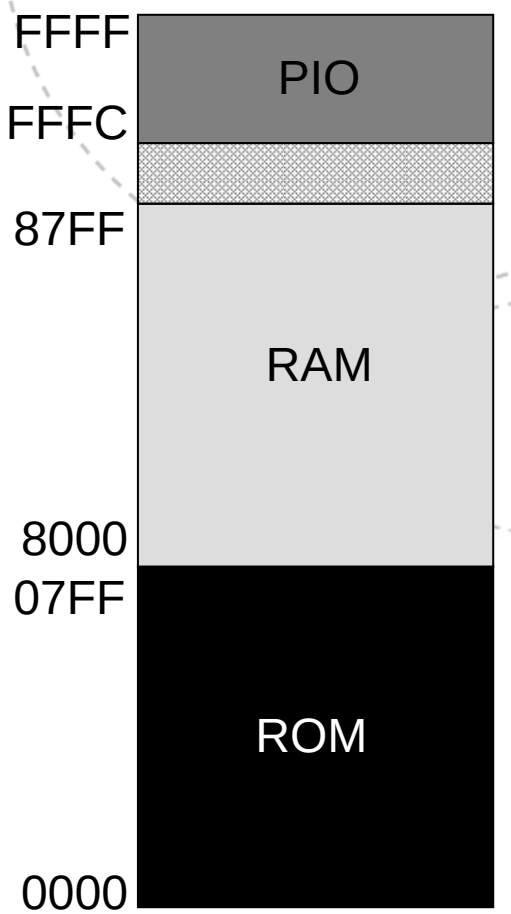
Dekod: 0000 0XXX XXXX XXXX

Høg: 0000 0111 1111 1111

0 7 F F

Låg: 0000 0000 0000 0000

0 0 0 0



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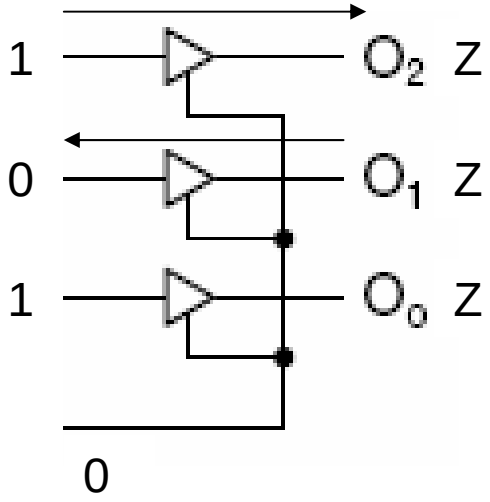
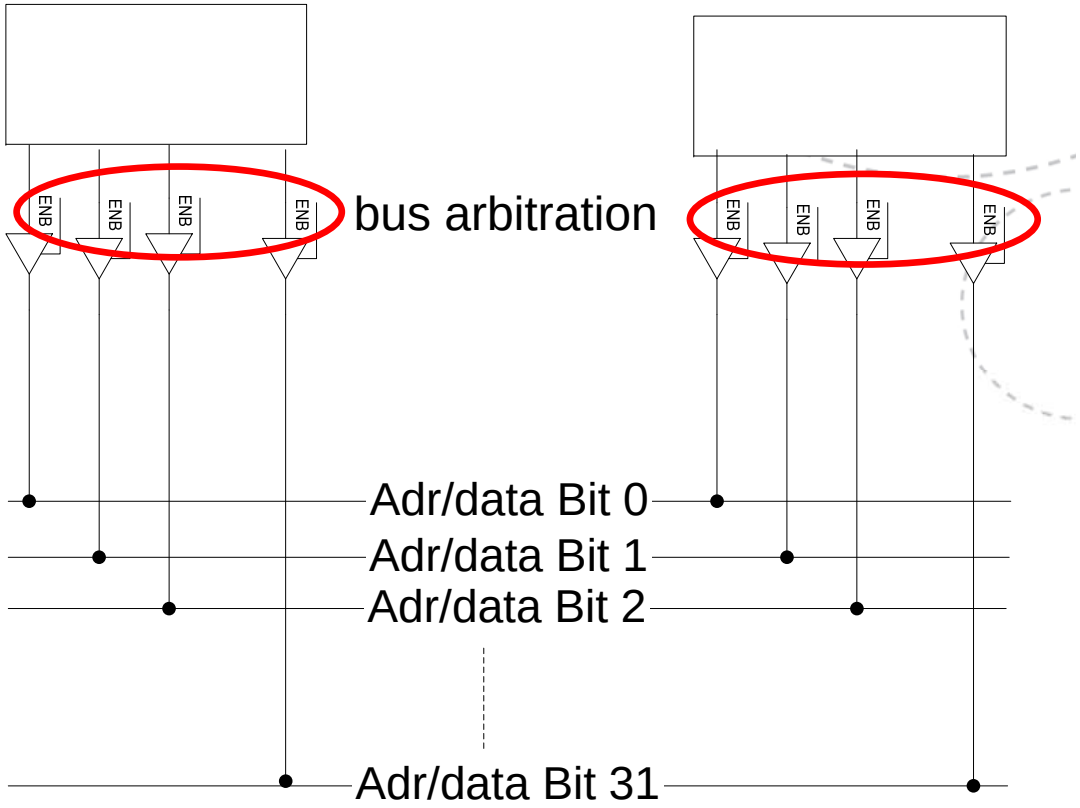
Three state buffer

- Buffer som gjer at ein kan kople frå f.eks. busslinjer
  - Tre pinnar
    - Inn
    - Ut
    - Kontroll
  - To tilstandar
    - Tilkopla
    - Høg impedans (three state)





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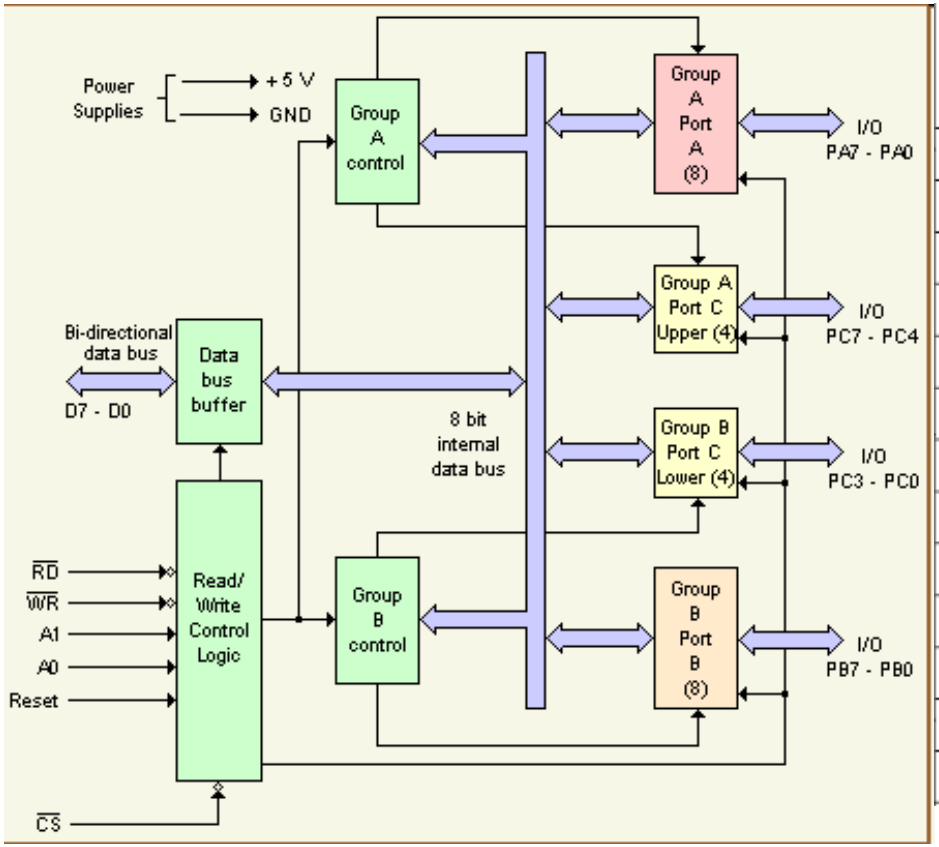
PIO (Parallel Input/Output) eks: Intel 8255

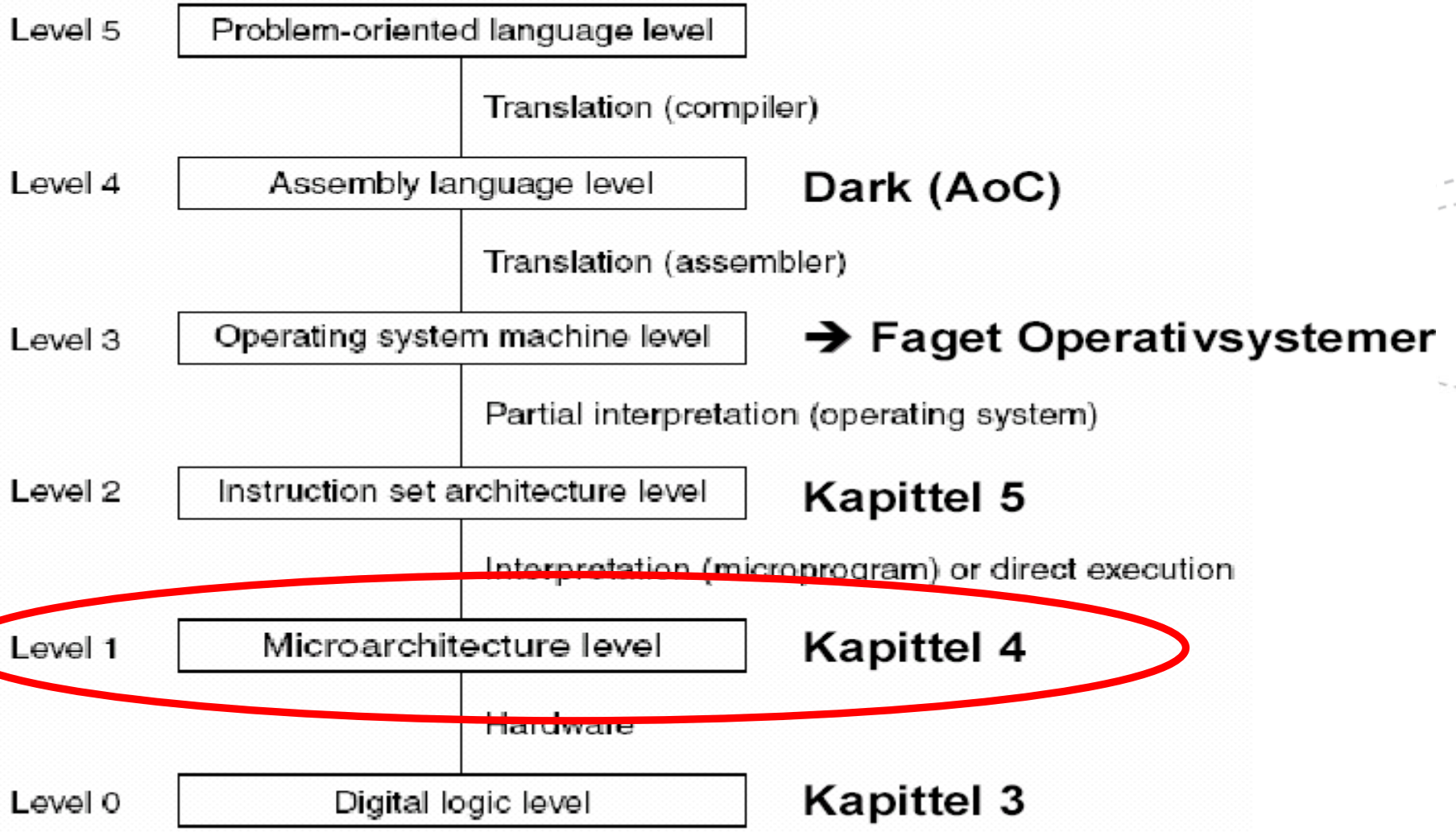


ADDRESS: These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

Kapittel 4: Microarchitecture level

Kapittel 4: Microarchitecture level



Kva er og Kva gjer

Spesifikasjon:
RISK
Superscalar
2 x ALU
Adreseringsmodi
:
Integer

Instruksjonssett:
ADD Rx Rx
LoadR mem, Rx
Store Rx, mem
:
:
AND Rx, Rx
SUB Rx, Rx