TDT4160
Datamaskiner Grunnkurs
2008

Gunnar Tufte

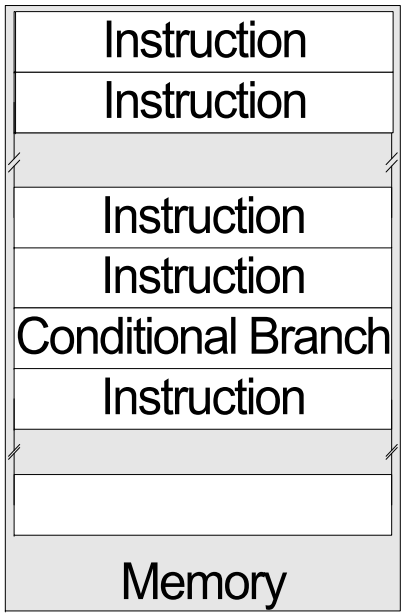
NTNU
Innovation and Creativity

I dag

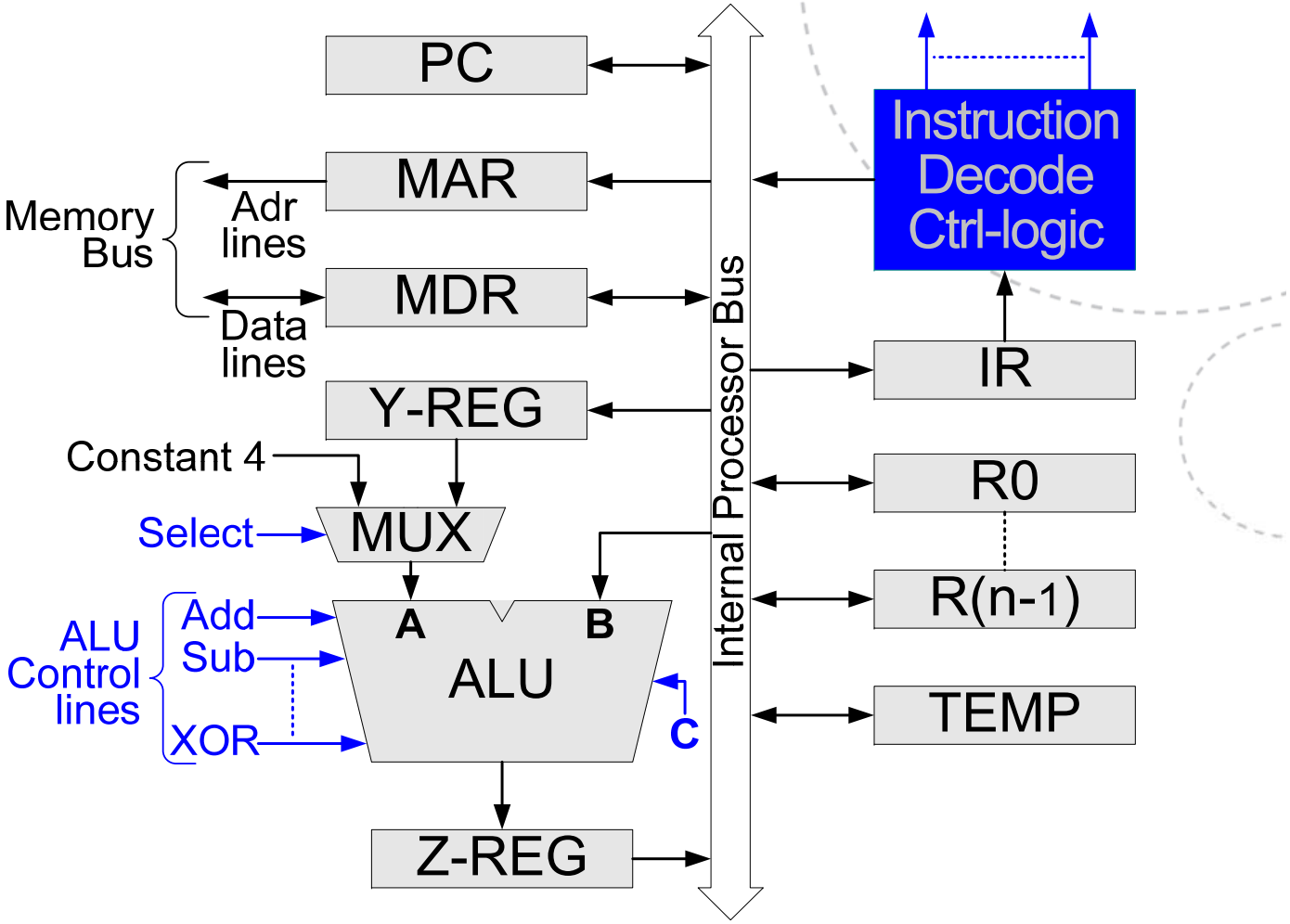
- Kva er inni 8051, P4 og UltraSparc
- Digital logic level (start kapitel 3)

- VIKTIG MELDING
  - Alle som har brukt NTNU-passord for AoC pålogging må skifte passord (NTNU-passord)
  - Meir info om dette, sjå it's learning

Skal sjå på Intel 8051, P4 and UltraSparc



Input/output



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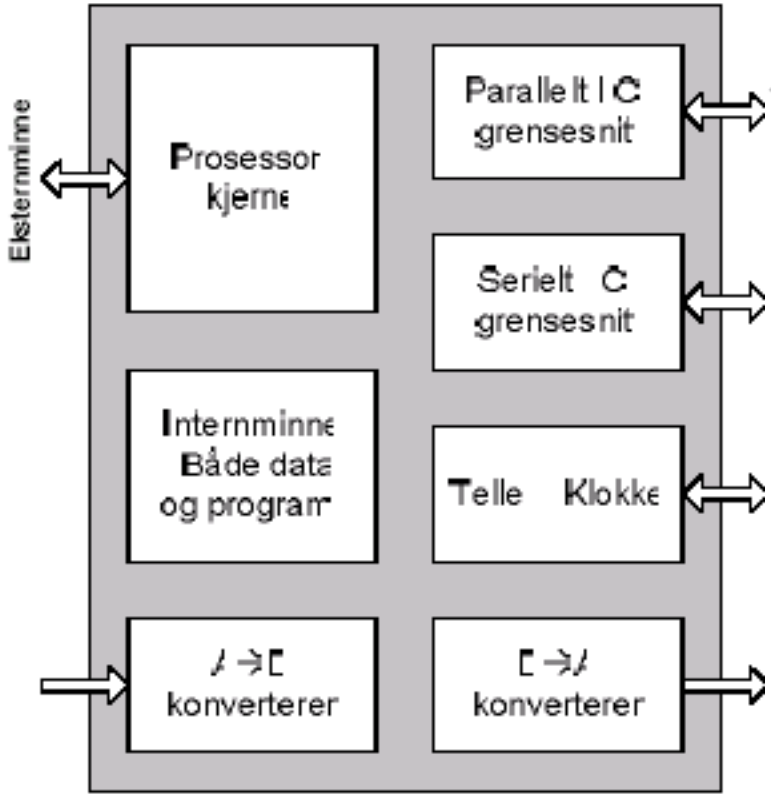
Intel 8051 mikrokontroller

8051

- Mikrokontroller
- Programvare er typisk fast og lagret i ROM
  - 8051: 4 KB
- ROM = Read Only Memory
- Lite, skrivbart minne
  - 8051: 128 bytes
- Treg men billig!



Intel 8051 mikrokontroller

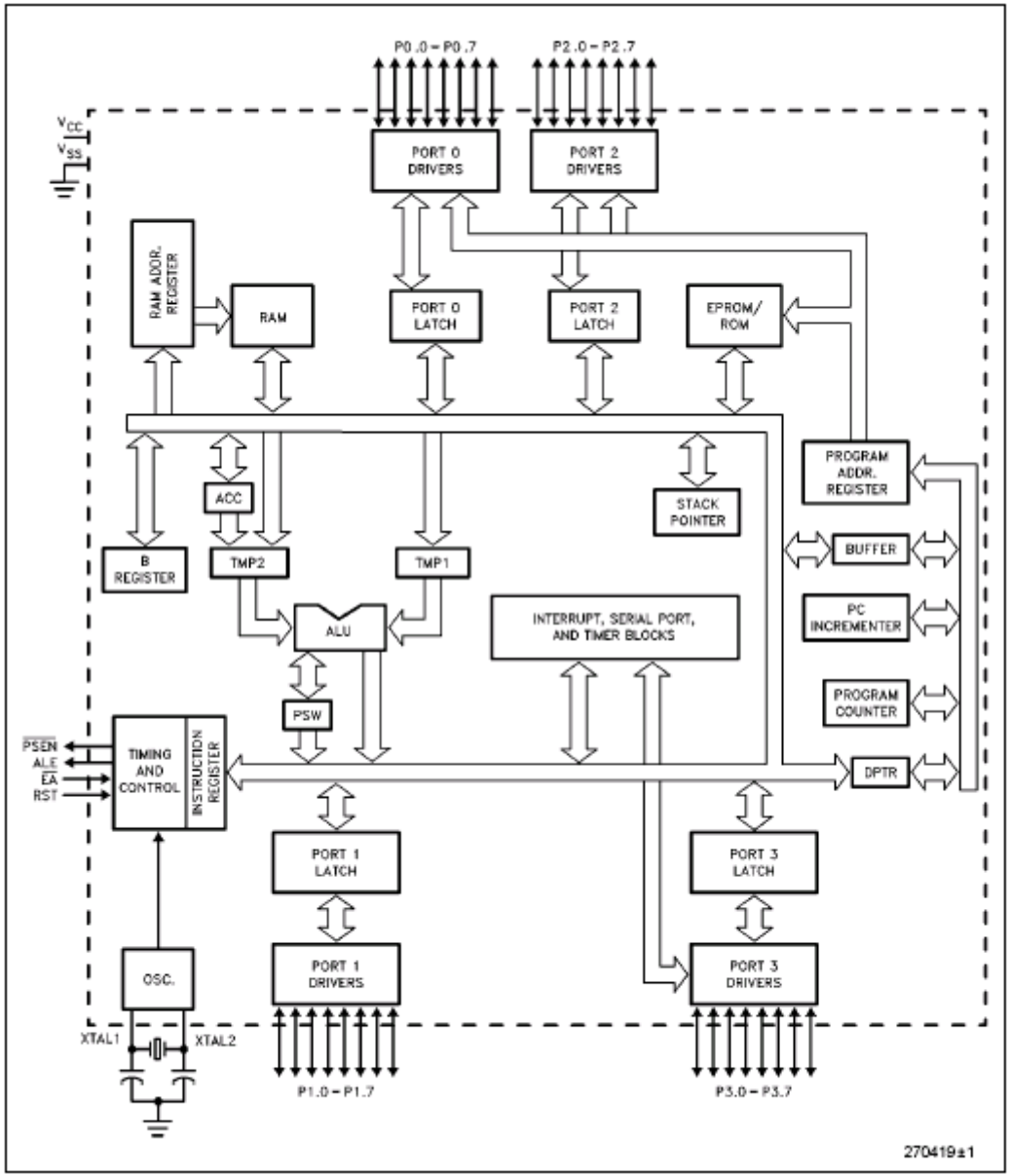


Figure 1. MCS® 51 Microcontroller Architectural Block Diagram

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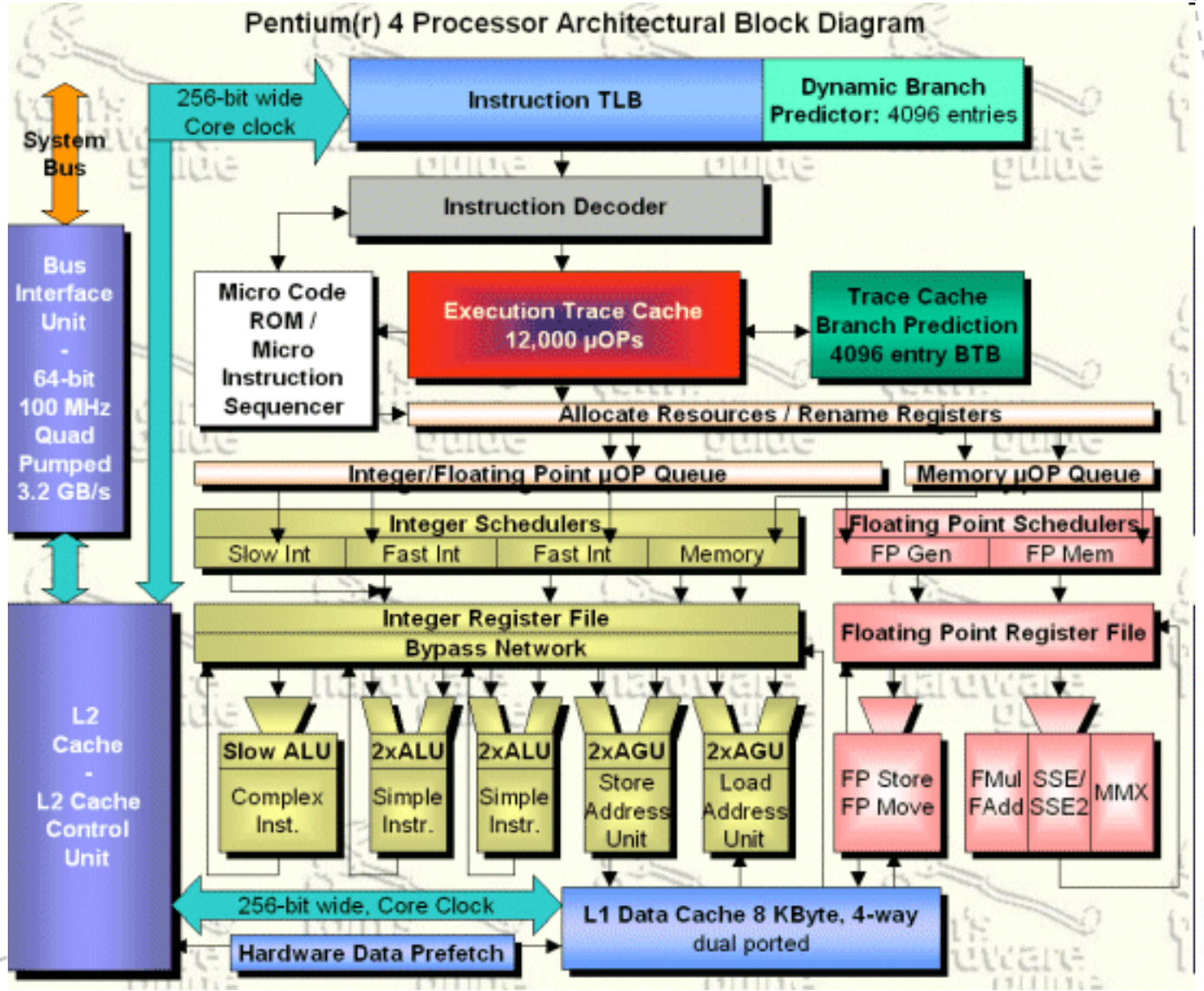
Pentium 4

- Intels nyeste og siste(?) x86-prosessor
  - Kan utføre programmer skrevet for 8086, 80286, ...
  - Intel derfor ikke fri til å lage en ny ISA, P4s ISA må omfatte alle instruksjoner fra eldre prosessorer
  - Men: Lavere nivåer er veldig annerledes
  - Oversetter x86-instr. til enklere instr. før utføring!
- Har nå fått problemer med varmeutviklingen
  - Mindre transistorer, større klokkefrekvens, mer strøm
  - 115 Watt på svært liten overflate
  - Dermed: Heller flere CPU på en chip enn raskere CPU

Pentium 4



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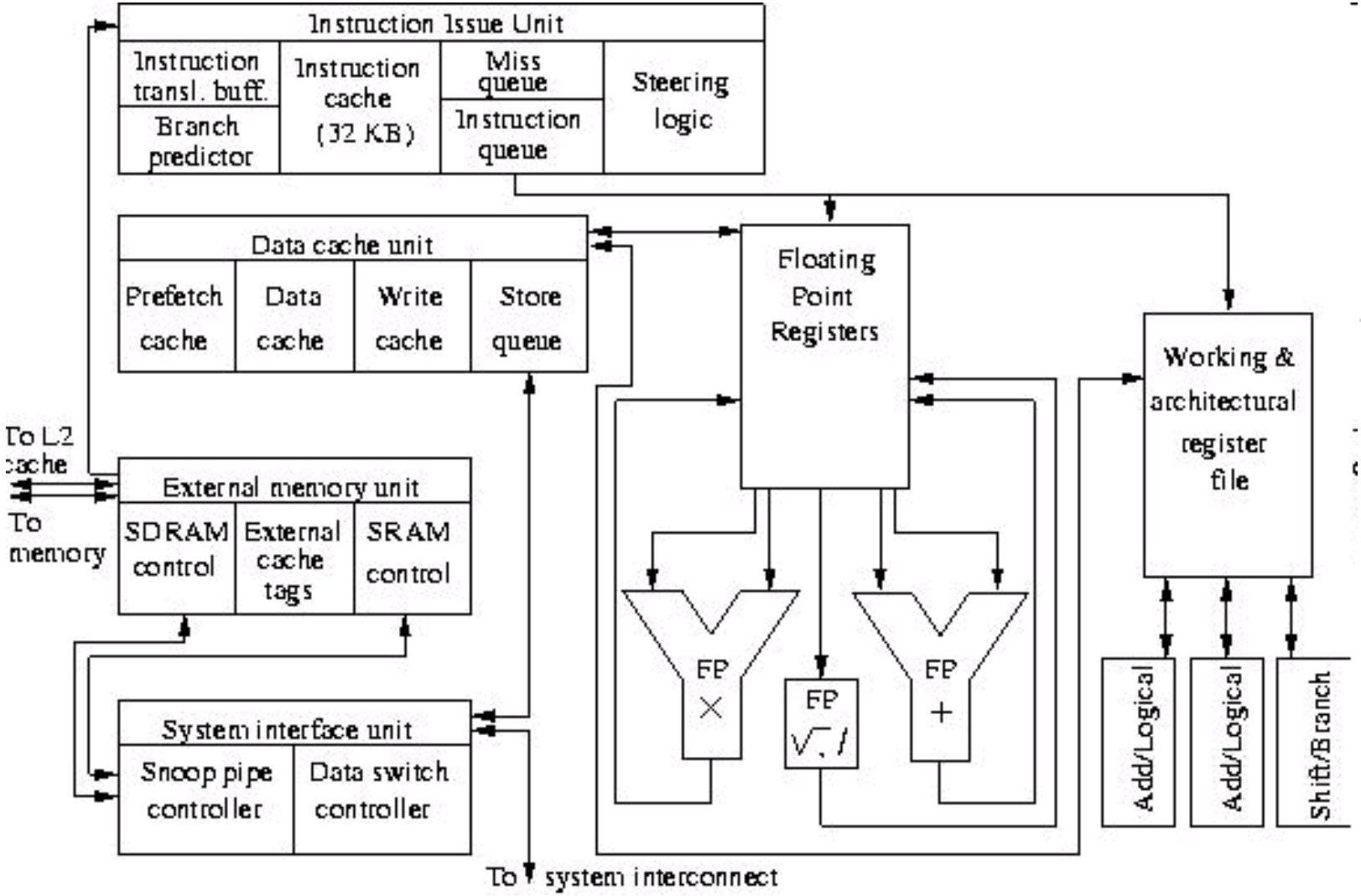
UltraSPARC III

- Fundamentalt annen ISA enn Pentium 4
  - RISC: Reduced Instruction Set Computer
  - P4 – CISC: Complex Instruction Set Computer
- Arkitektur laget av Sun Microsystems (1987)
  - Selve brikkene produsert av andre
- UltraSPARC er 64 bits prosessor
  - 64 bits registre
  - ALU utfører beregninger på 64 bit i slengen
  - 64 bits adresser til minne

UltraSPARC III



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P4, UltraSparc III og 8051

- P4 og UltraSPARC III
  - Superscalar
    - Mange pipelines
    - Seperat integer og flyttal einheitar
    - Djupe pipelines
  - Mange eksterne Adr/data pinnar
    - Kan adressere heile ord
    - Seperat data / adresse buss
  - Cache
    - L1, L2, insruksjon, data
  - Avansert kø for instruksjonsutførelse
    - Branche predictor
    - Out of order insruction execution
  - **Kraftig, stor, dyr, komplisert, stort effektforbruk**
- 8051
  - Enkel arkitektur
    - Ein / ingen pipeline
    - Ikkje flyttal
  - Lite adresse område
    - Delt adr/data buss
    - Adresserar 8 eller 4 bit
  - Generelle portar
    - Fleksibelt grensesnitt
  - Treg, liten, enkel, lite effekt forbruk

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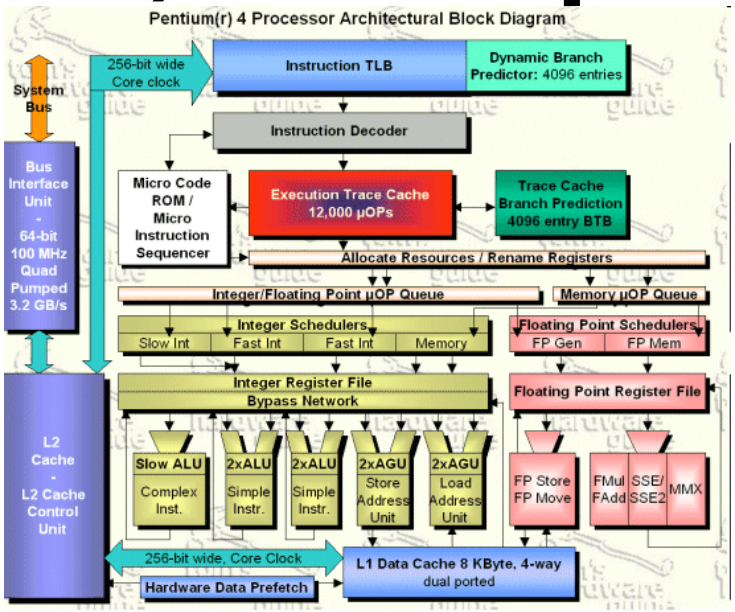
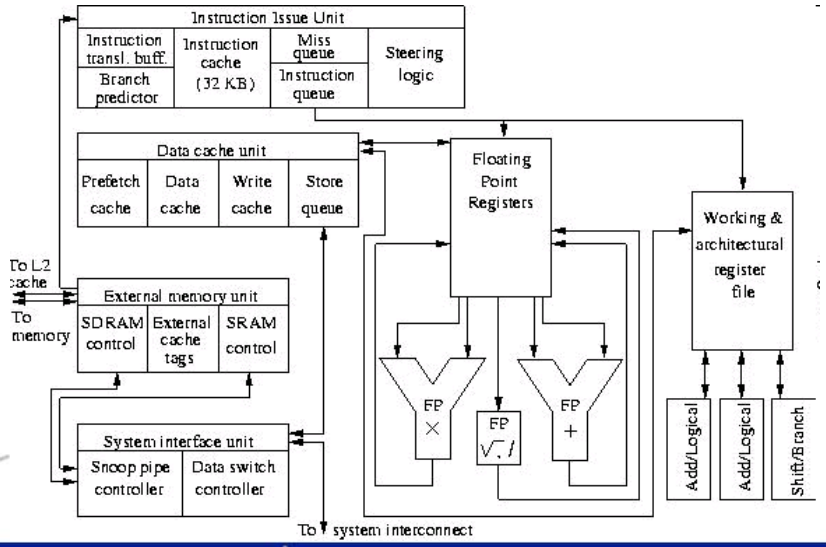
P4, UltraSparc III og 8051





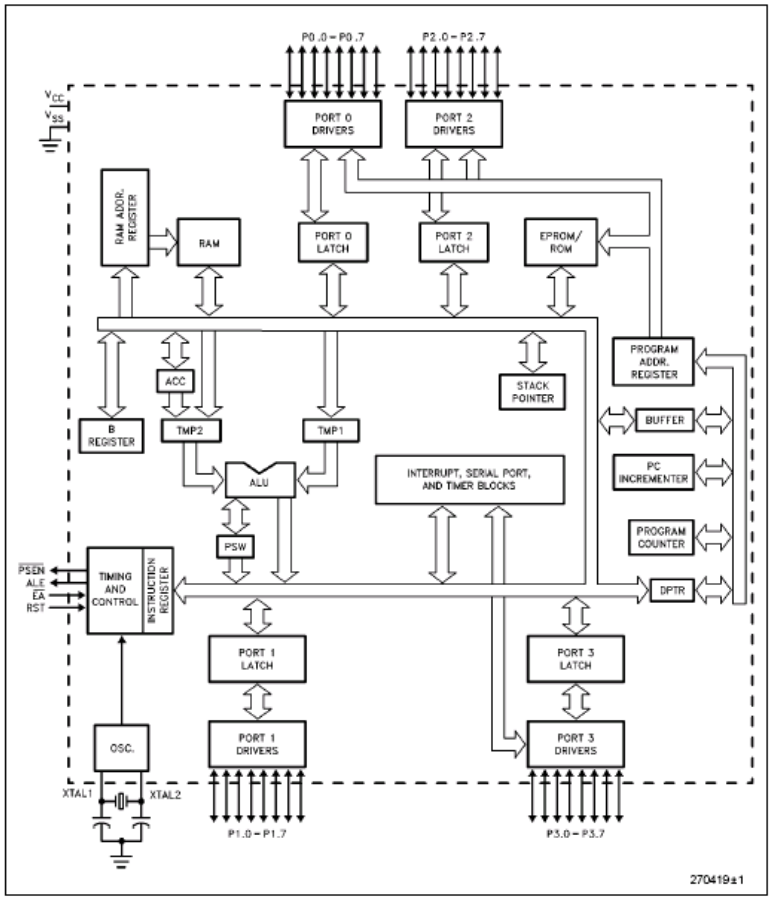


Figure 1. MCS® 51 Microcontroller Architectural Block Diagram

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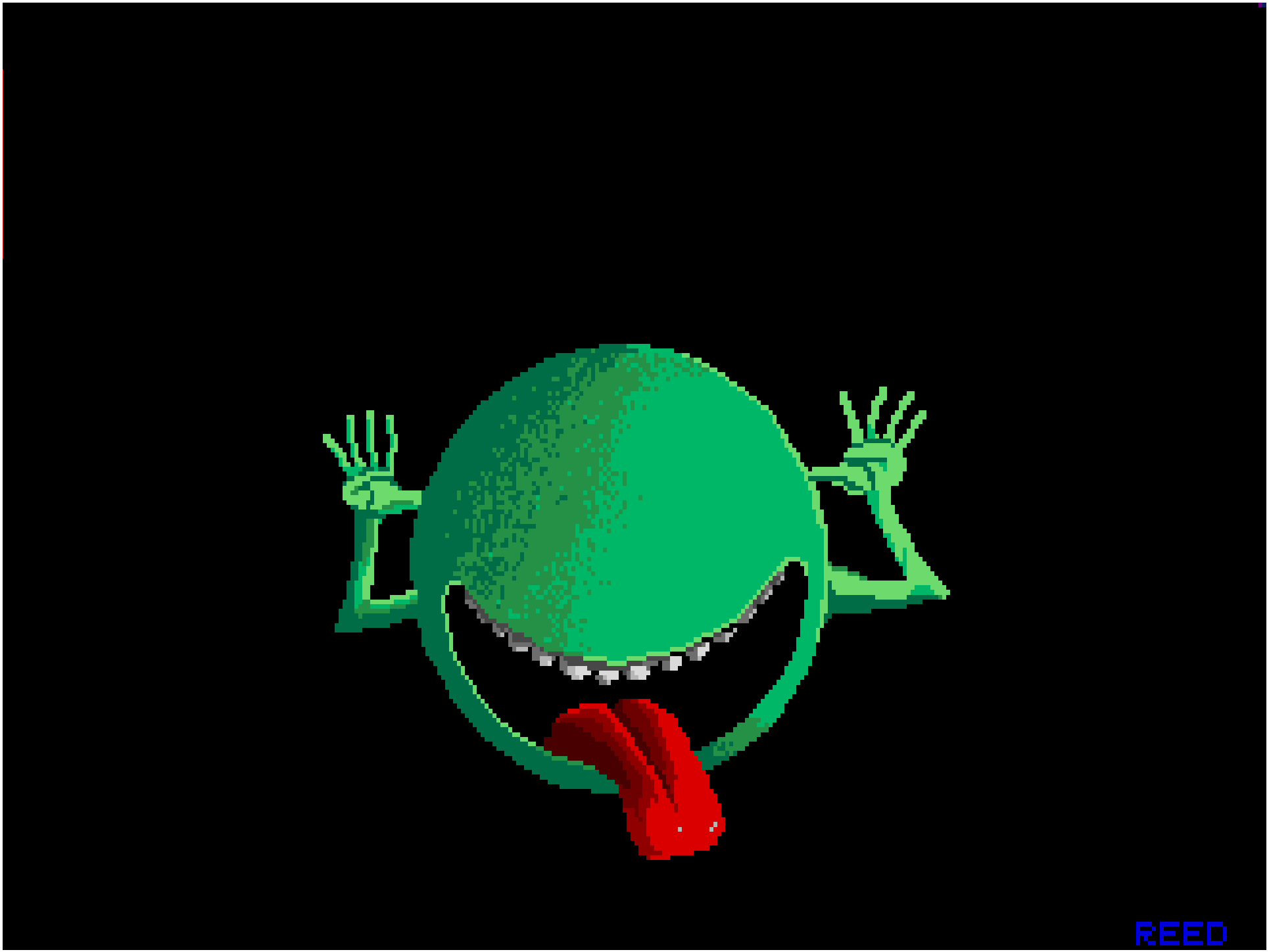
REED

Liten test 1

- Kva nytt var det von Neumann arkitekturen innførte?
  - A: Hierarki i minne (Memory hierarchy")
  - B: Program lagra i minne ("stored program computer")
  - C: Høgnivå programmeringsspråk
- Kva komponent(ar) er ein del av prosessorens "datapath"
  - A: ALU og Register,
  - B: Kontrolleinheit
  - C: Program Counter registeret (PC) og Instruksjons registeret (IR)
- Kvar ligg i program teljar registeret (PC)
  - A: Adresse til instruksjon
  - B: Nummeret på instruksjonen som utføres
  - C: Peikar til dataminne
- Kva antal instruksjonar kan ein prosessor med eit 3 stegs samlebånd "pipline" utføre kvar klokkeperiode (max)?, kva med 5 steg?
  - A: 1 instruksjon kvar klokkeperiode i begge tilfella
  - B: 3 instruksjonar for 3 steg og 5 instruksjonar for 5 steg
  - C: 3 instruksjonar for 3 steg og 5/3 instruksjonar for 5 steg

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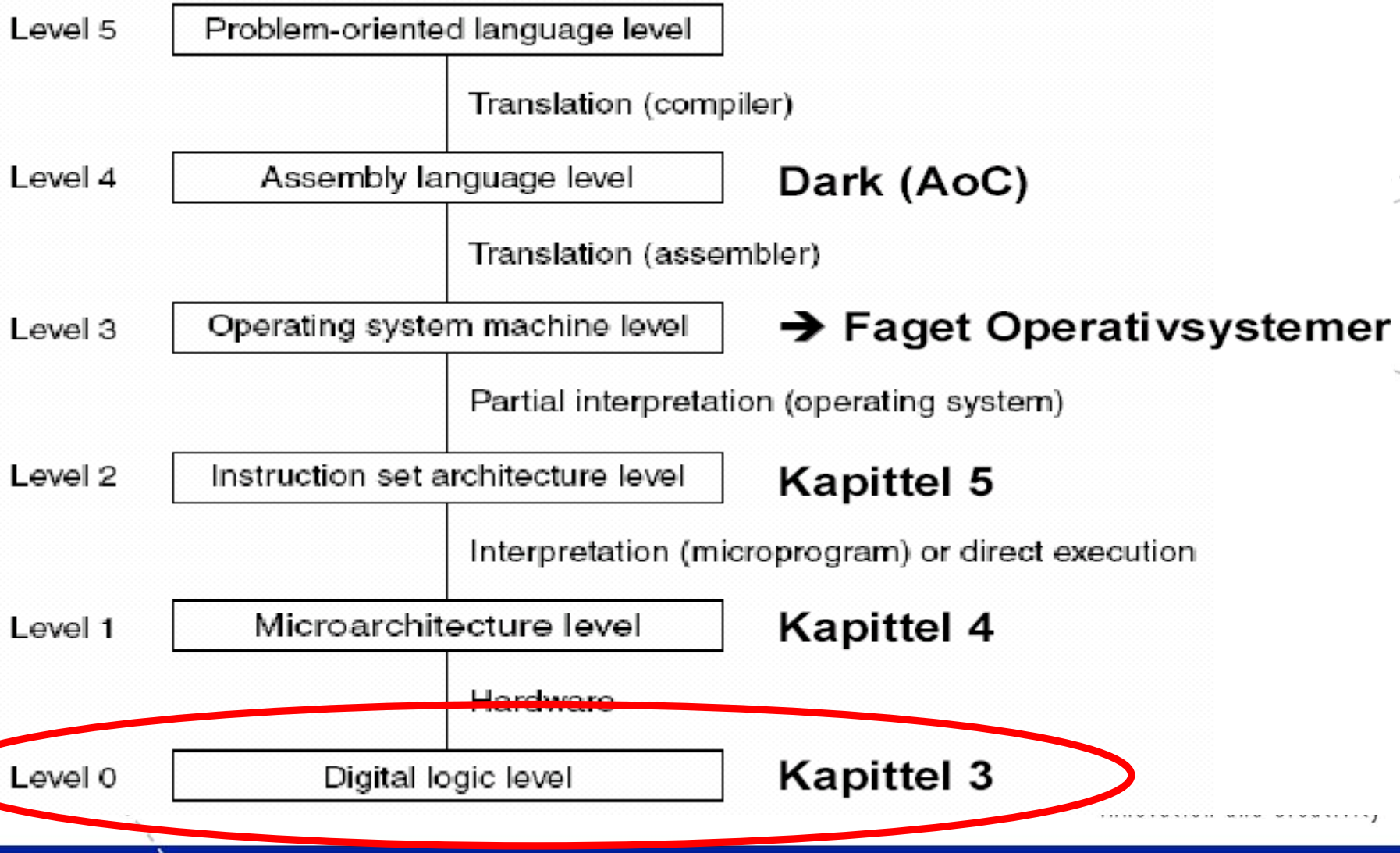
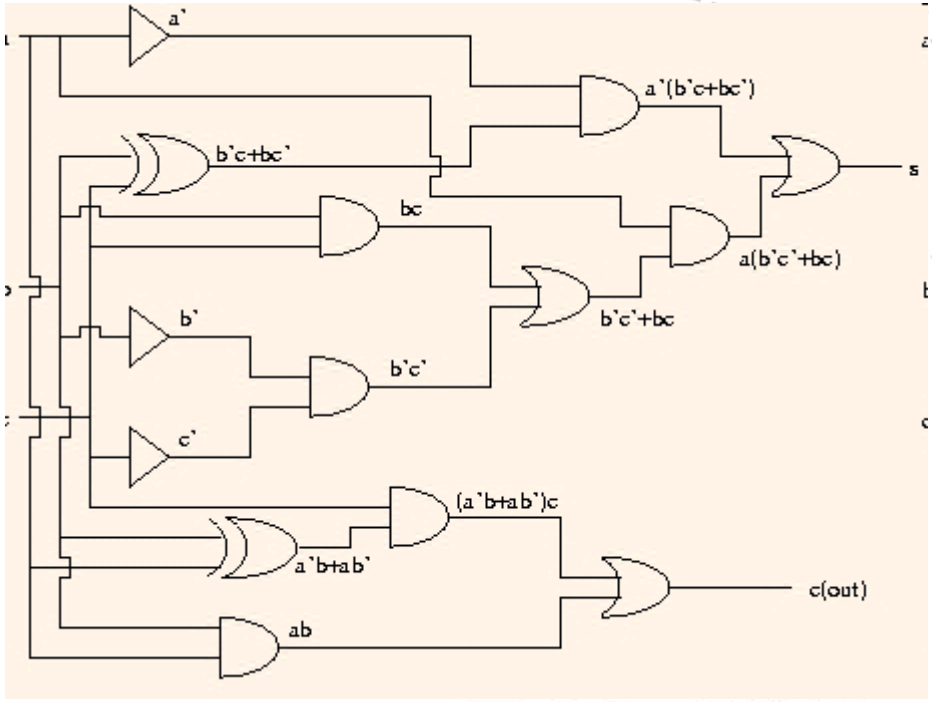
Kapittel 3: Digital logic level



Nivå 0: Digtalekretsar

- Fundamentale komponentar
  - AND, OR, NOT,NAND, NOR XOR porter
  - D-vipper for lagring av ett bit
- Samansette komponentar
  - Aritmetiske kretsar –
    - adderere, skiftere, …
  - Dekodere
  - Multiplekser
  - Registre
    - 8, 16, 32, 64 vipper



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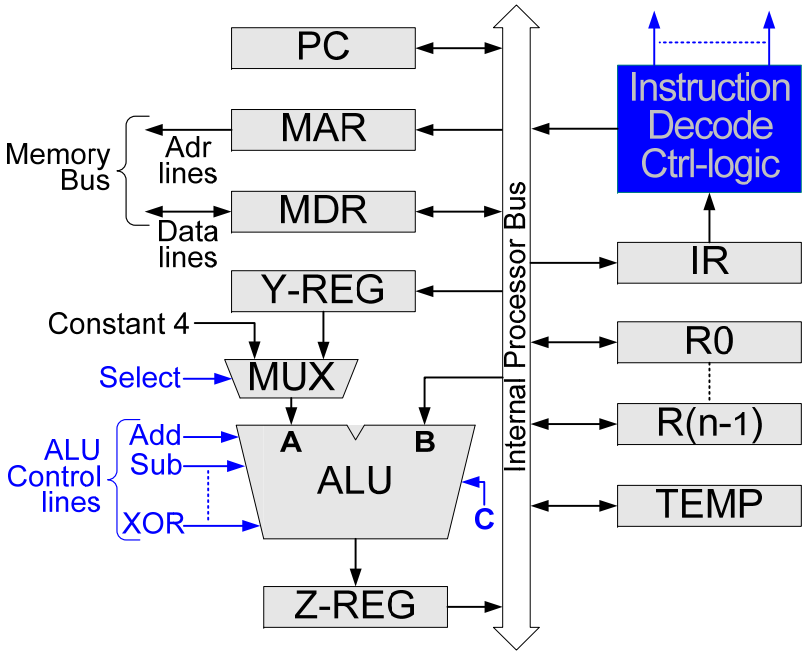
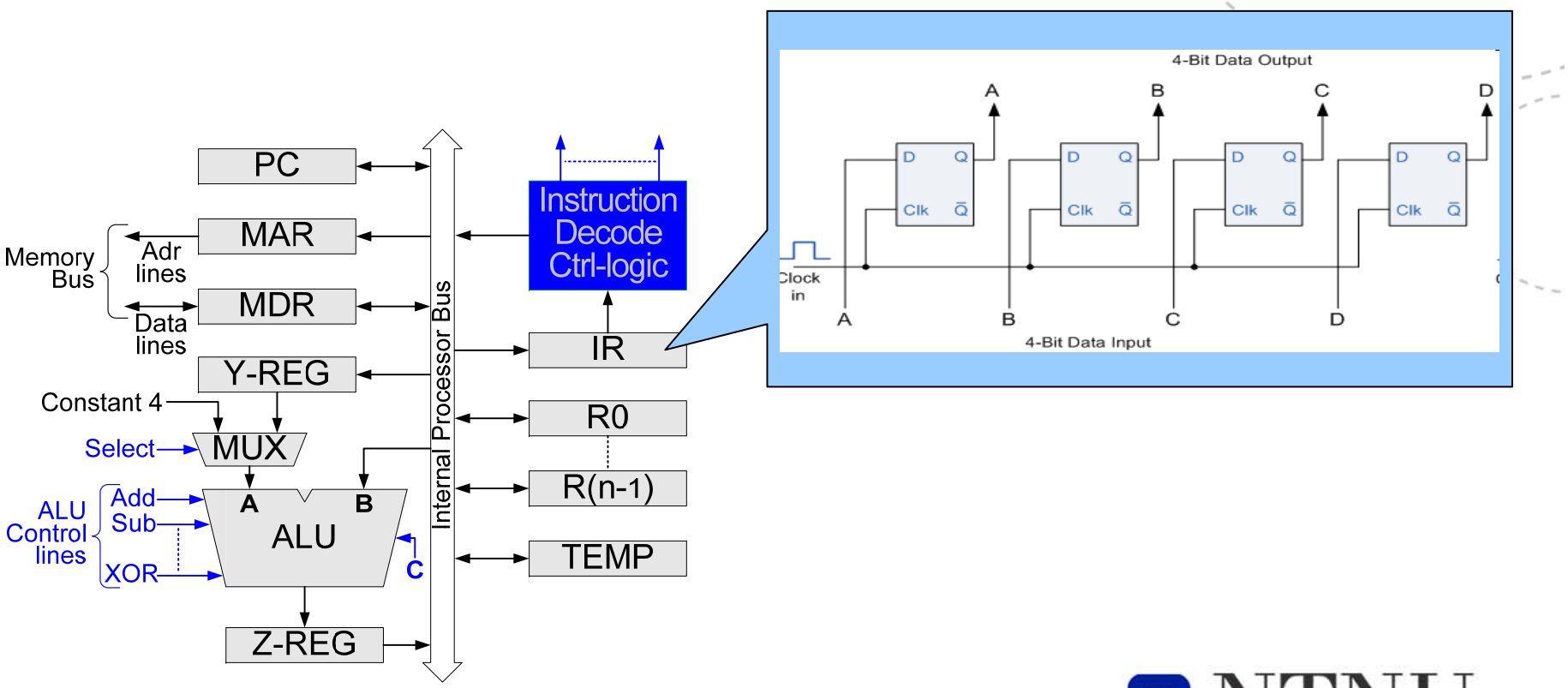
Digital logic level

- Kva og korleis



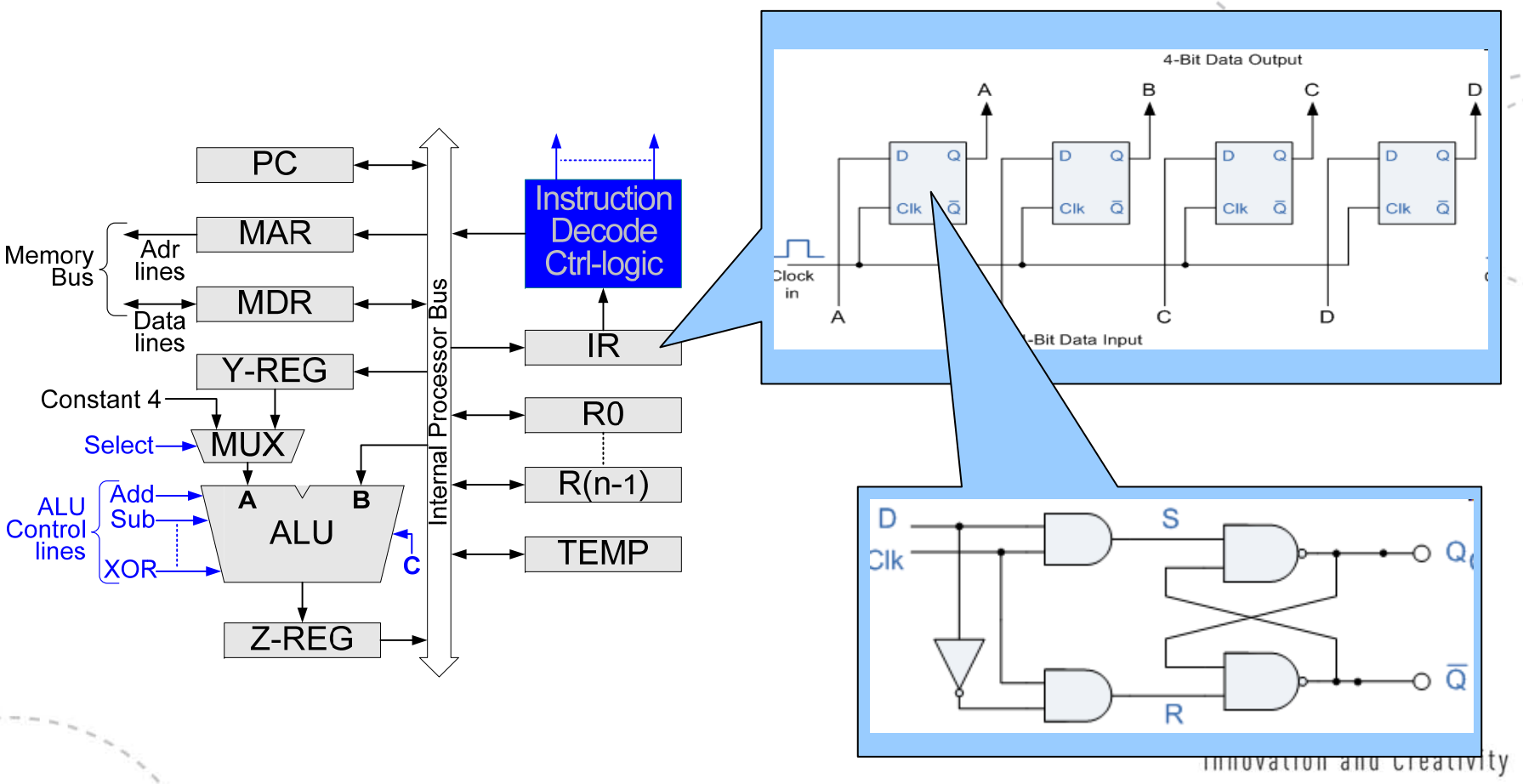
Digital logic level

- Kva og korleis



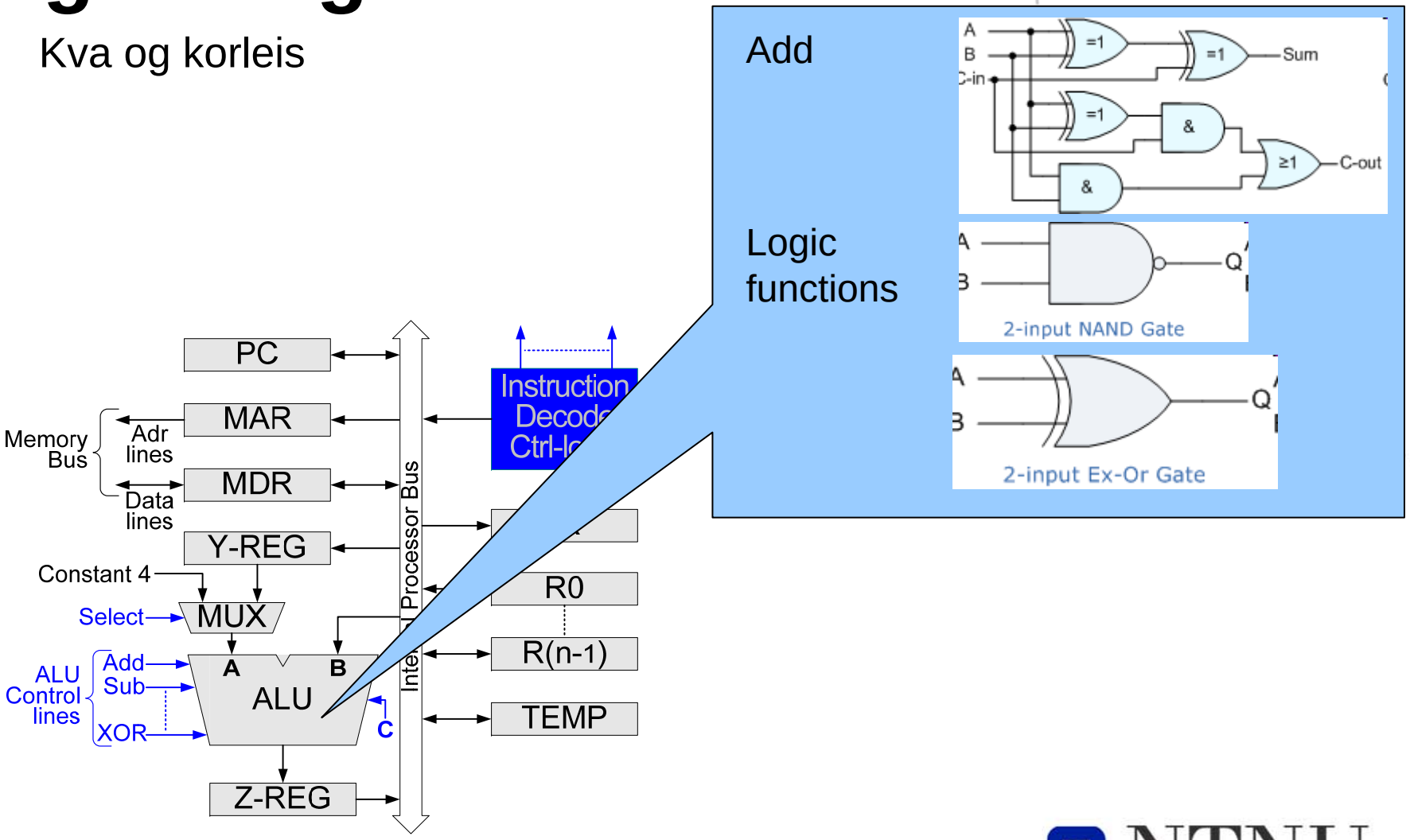
Digital logic level

- Kva og korleis



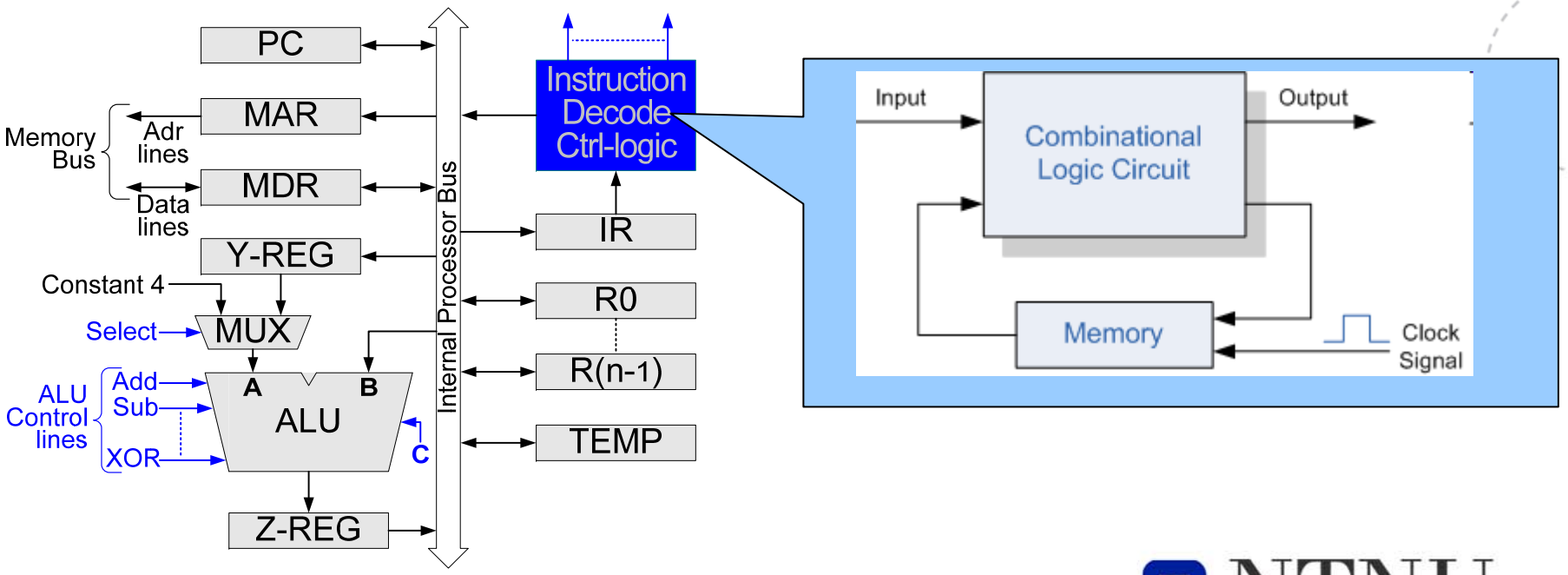
Digital logic level

- Kva og korleis



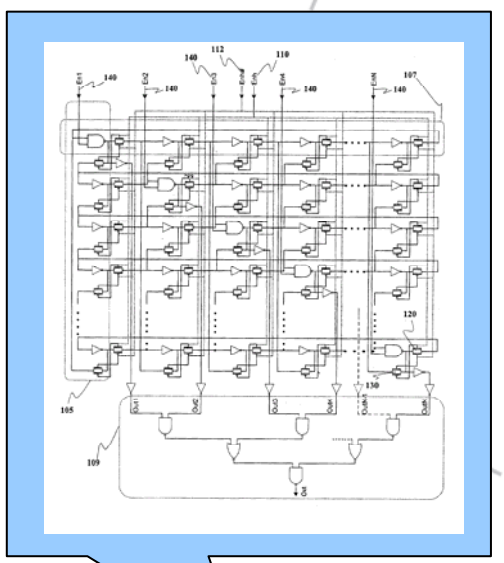
Digital logic level

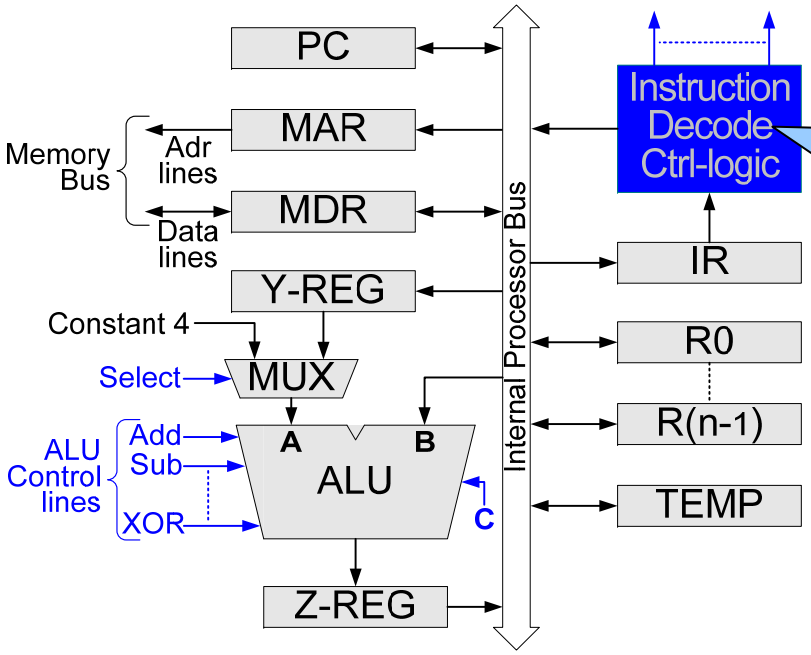
- Kva og korleis

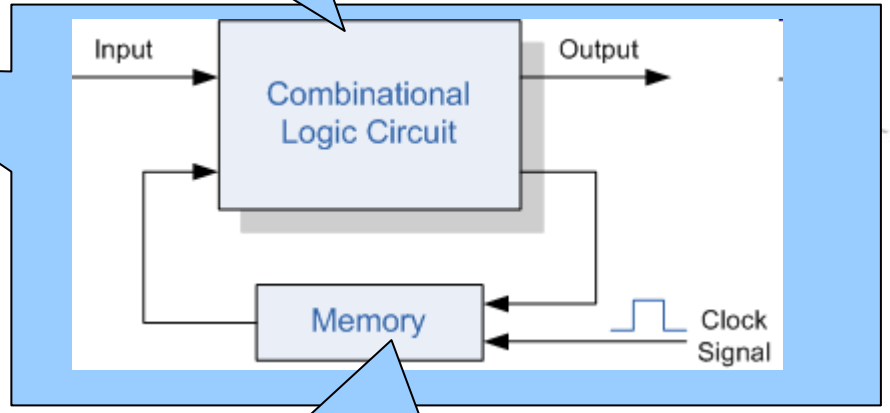


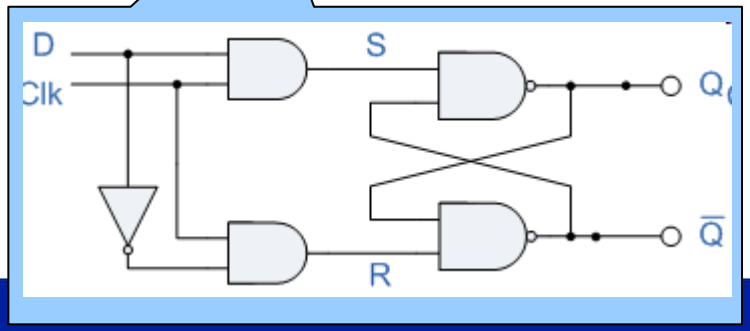
Digital logic level

- Kva og korleis



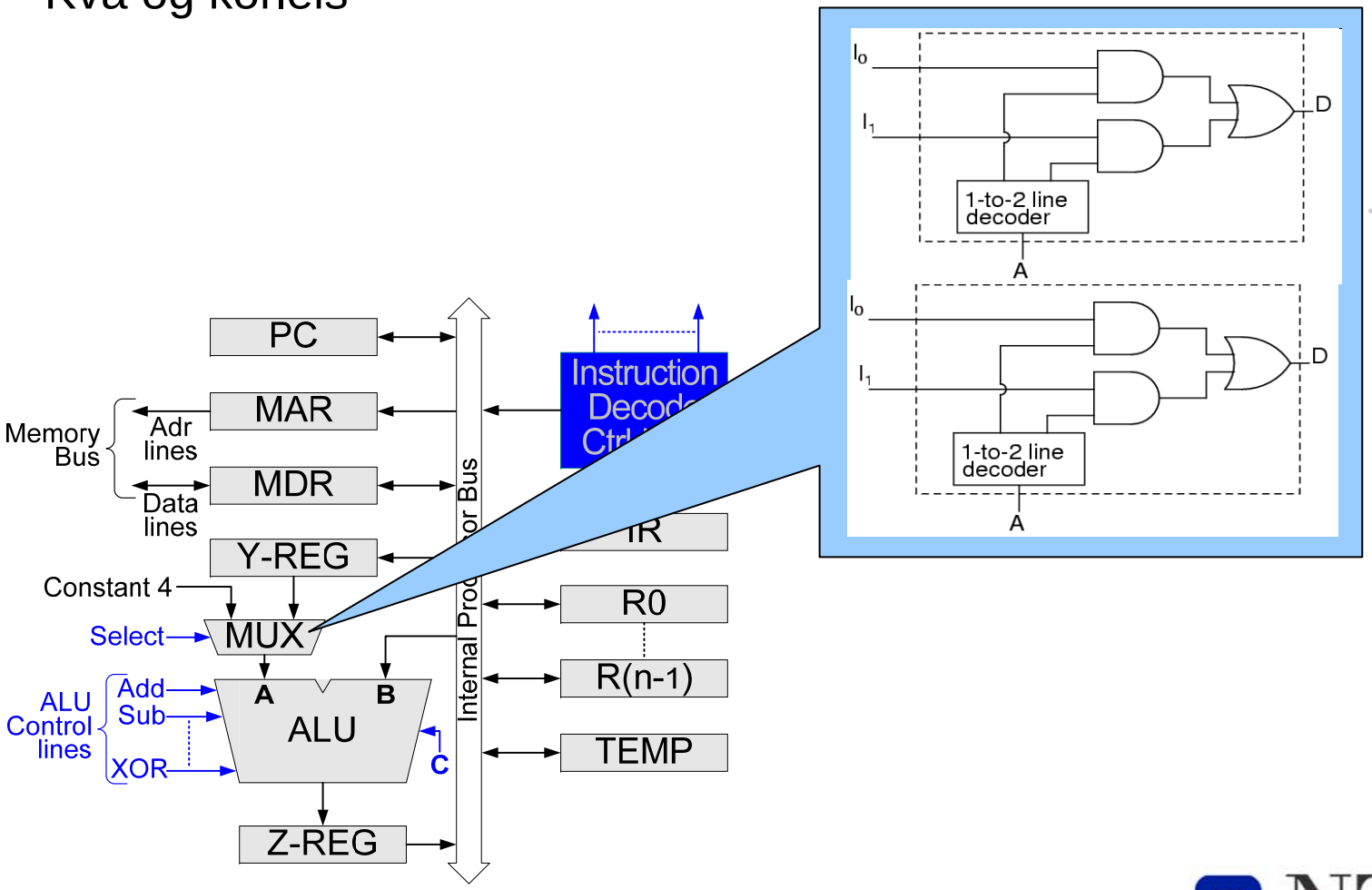






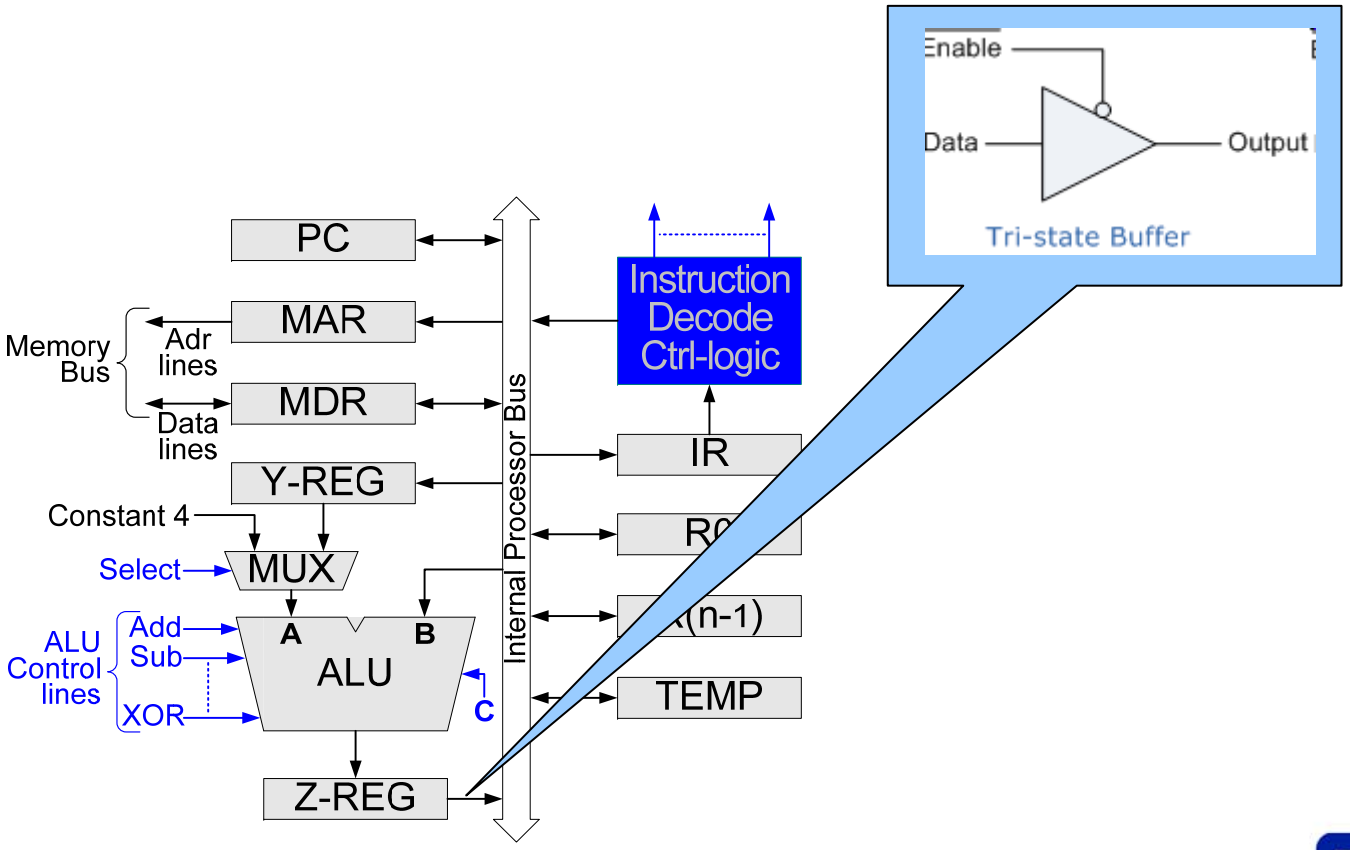
Digital logic level

- Kva og korleis



Digital logic level

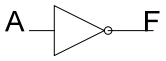
- Kva og korleis



Kort repetisjon 3.0 -> 3.3.4

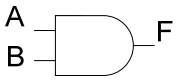
- Logisked portar

NOT



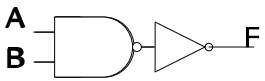
A	F
0	1
1	0

AND



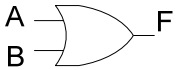
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND



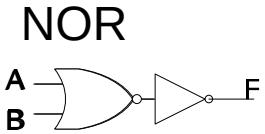
A	B	F
0	0	
0	1	
1	0	
1	1	

OR



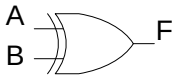
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

NOR



A	B	F
0	0	
0	1	
1	0	
1	1	

XOR



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

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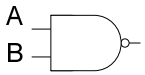
Kort repetisjon 3.0 -> 3.3.4

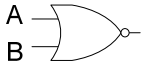
- Har no byggeklossar til å lage alle bolskefunksjonar

NAND

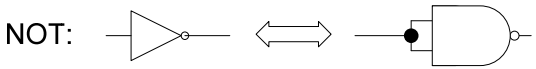


A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

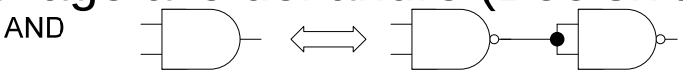
NOR

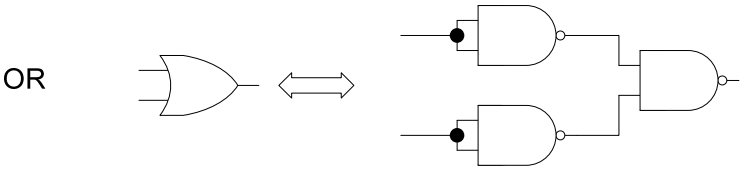


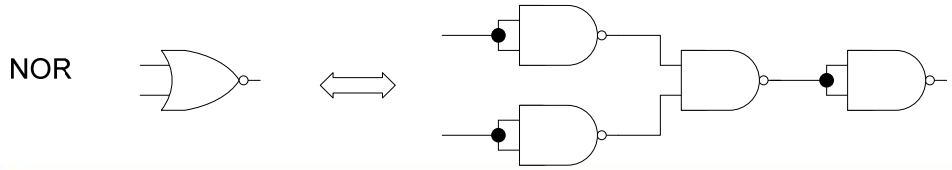
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



- Kan no lage alle dei andre (Boolsk algebra)







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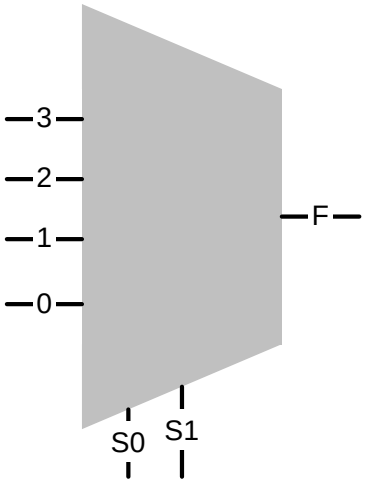
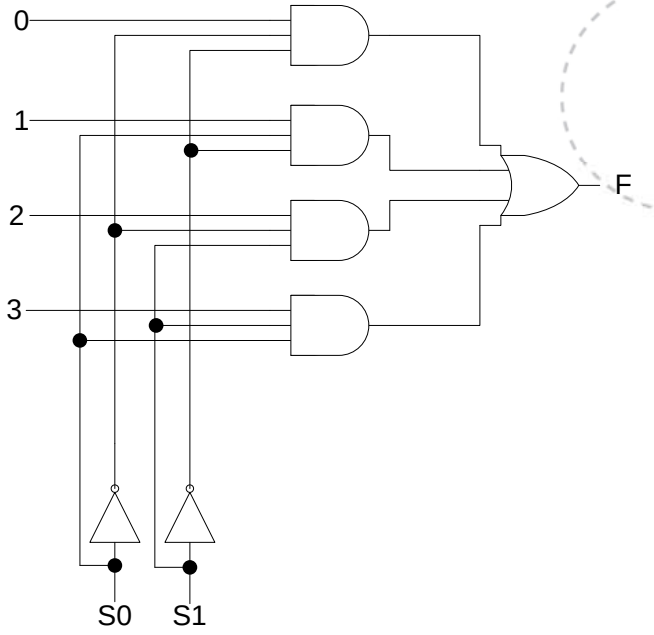
Kort repetisjon 3.0 -> 3.3.4

- Kan lage kombinatoriske kretsar
  - Kretsar uten klokke eller sekvensielle eigenskapar
    - Decoders
    - Encoders
    - Multiplexers
    - Binary Adders
    - Binary Subtractors

- Eksempel kretsar: Multiplexer



S1	S0	F
0	0	inn 0
0	1	inn 1
1	0	inn 2
1	1	inn 3



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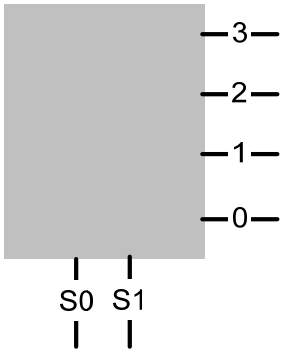
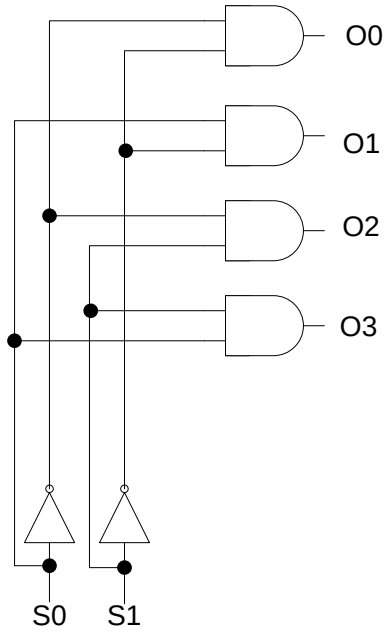
Kort repetisjon 3.0 -> 3.3.4

- Kan lage kombinatoriske kretsar
  - Kretsar uten klokke eller sekvensielle eigenskapar
    - Decoders
    - Encoders
    - Multiplexers
    - Binary Adders
    - Binary Subtractors

- Eksempel kretsar: Decoder



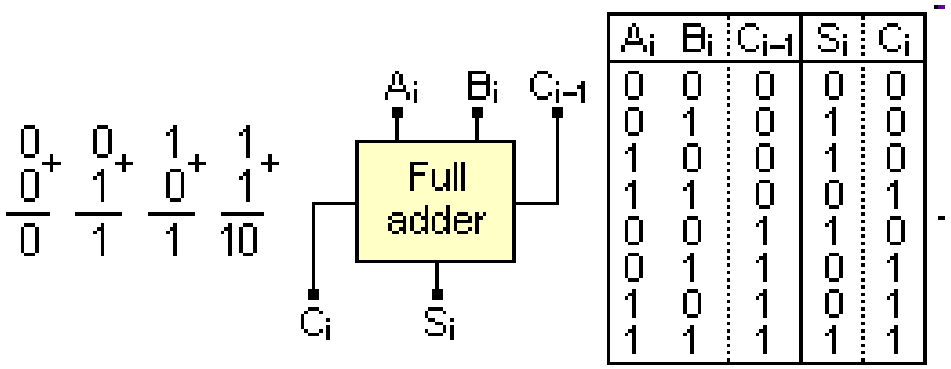
S1	S0	O3	O2	O1	O0
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



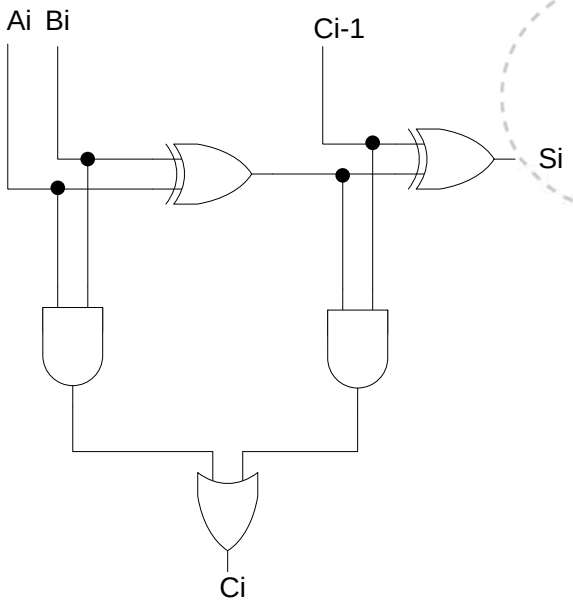
Kort repetisjon 3.0 -> 3.3.4

- Kan lage kombinatoriske kretsar
  - Kretsar uten klokke eller sekvensielle eigenskapar
    - Decoders
    - Encoders
    - Multiplexers
    - Demultiplexers
    - Binary Adders
    - Binary Subtractors

- Eksempel kretsar: Full adder



A_i	B_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1



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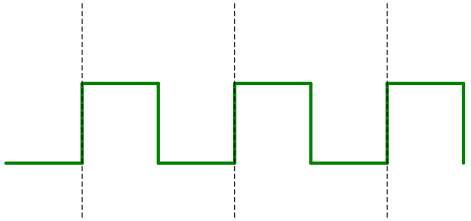
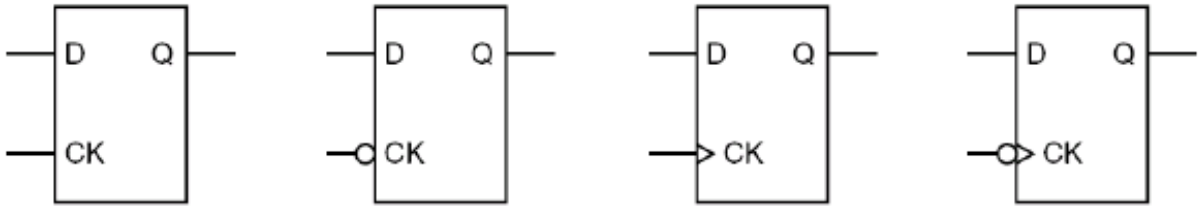
Kort repetisjon 3.0 -> 3.3.4

- Sekvensiellekretsar
  - Kretsar med minne neste tilstand kan vere avhengig av tidligare tilstand (klokke og lager)
    - Minne (register)
    - Teljarar
    - Tilstandsmaskiner
- Eksempel kretsar: D-vippe (D latch) og Flip-flop

  Lagrer en bit, basis byggekloss for minne

  a) D-vippe, lagrer D når CK = 1
  b) D-vippe, lagrer D når CK = 0
  c) D-flip-flop, lagrer D på stigende klokkeflanke (0➔1)
  d) D-flip-flop, lagrer D på synkende klokkeflanke (1➔0)





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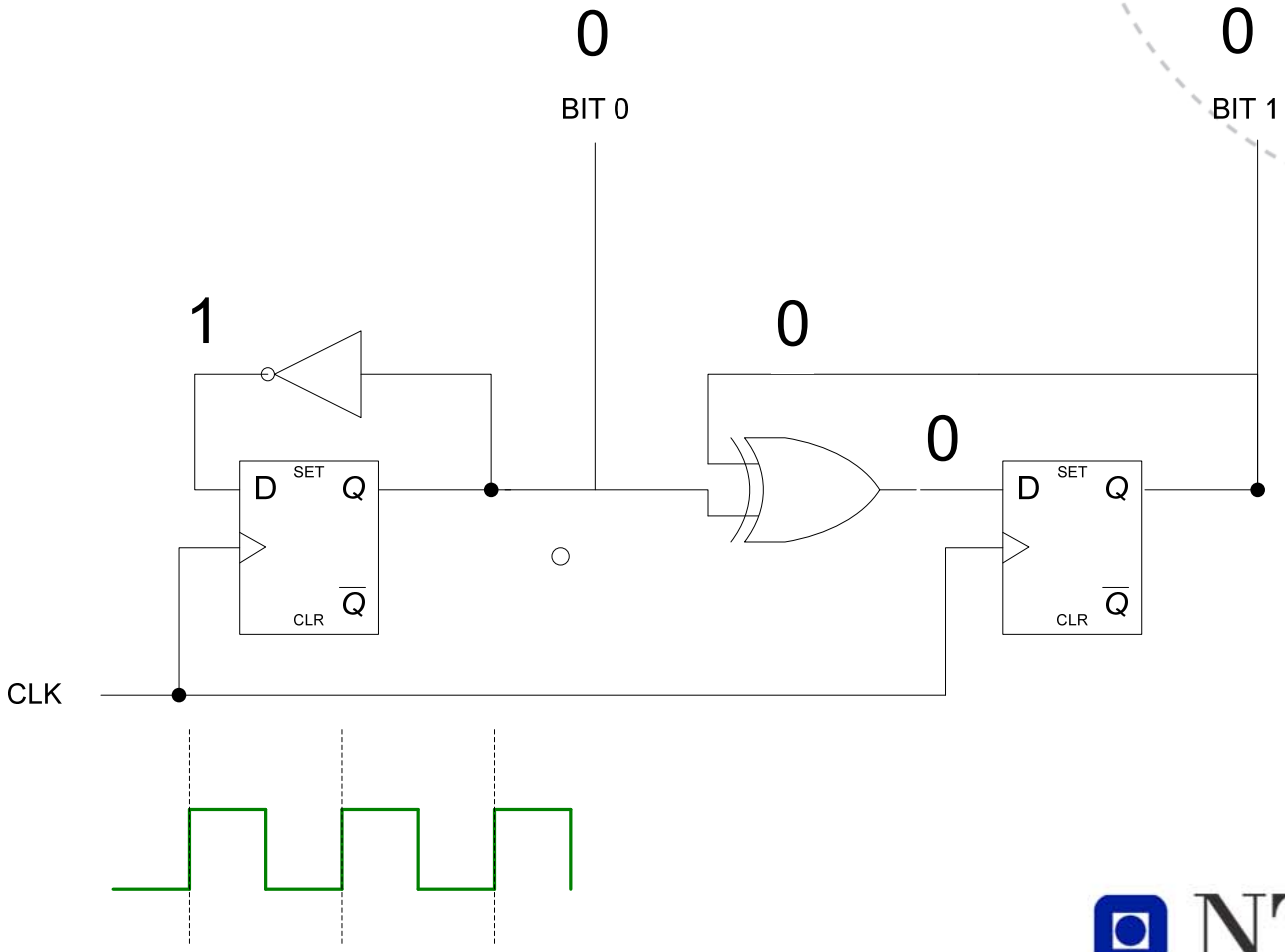
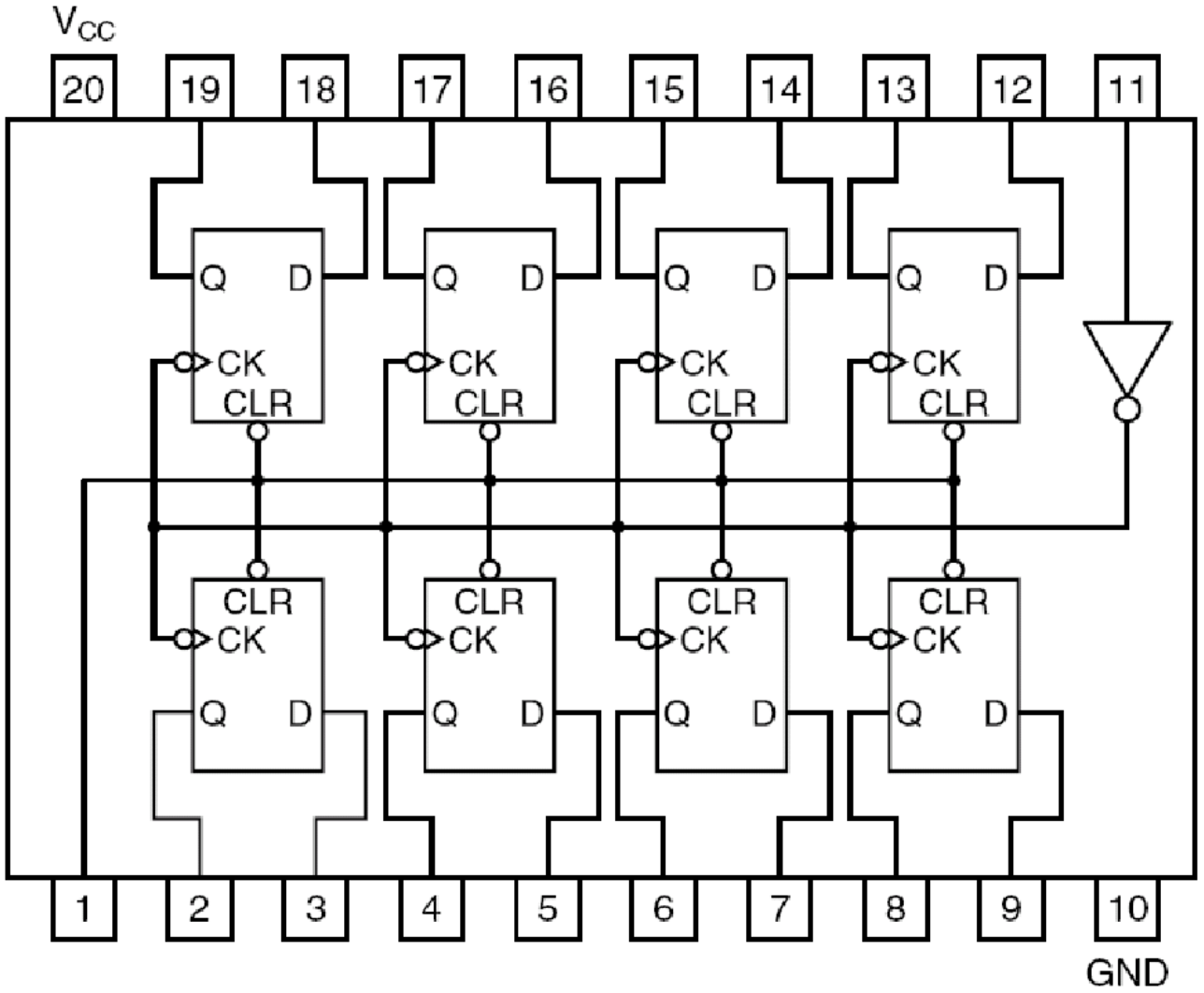
Kort repetisjon 3.0 -> 3.3.4

- Eksempel kretsar: 2-bits teljar (sekvensielkrets)



Minne kretsar no er me på 3.3.4

- Eksempel krets: 8-bits minnebrikke



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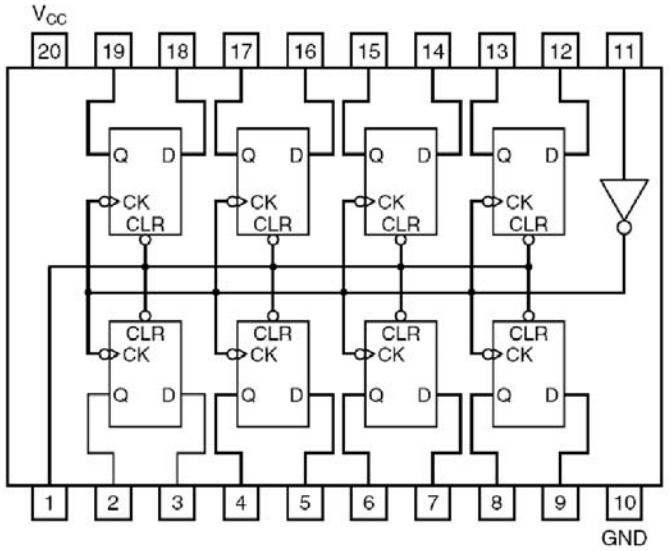
8-bits minnebrikke

- Upraktisk organisering
  - 20 pinner for 8 bit lagringskapasitet
- Hva da med hovedlager på 1GB?
  - 21 474 836 480 pinner…
- Kva kan vi gjøre?
  - Trenger ikke uavhengig tilgang til alle bit
  - Trenger ikke samtidig tilgang til alle bit



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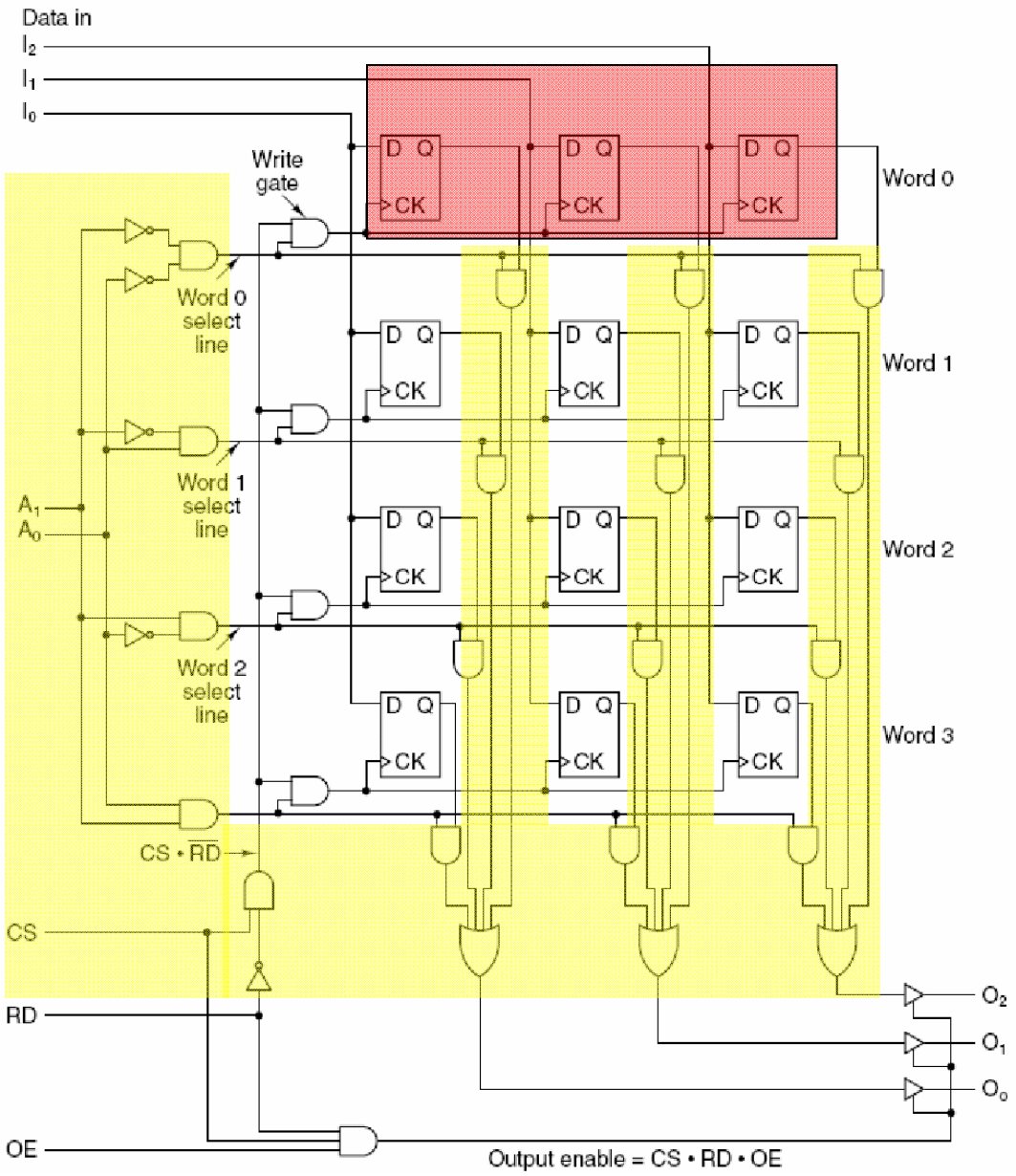
4 x 3 bit minne (4 ord på 3 bit)



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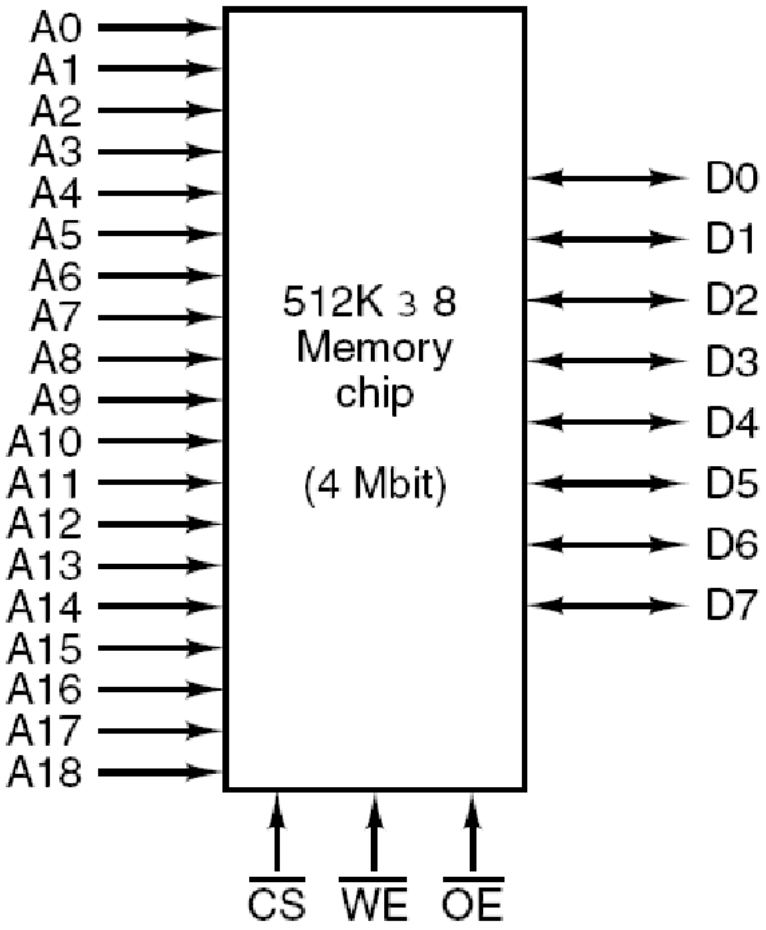
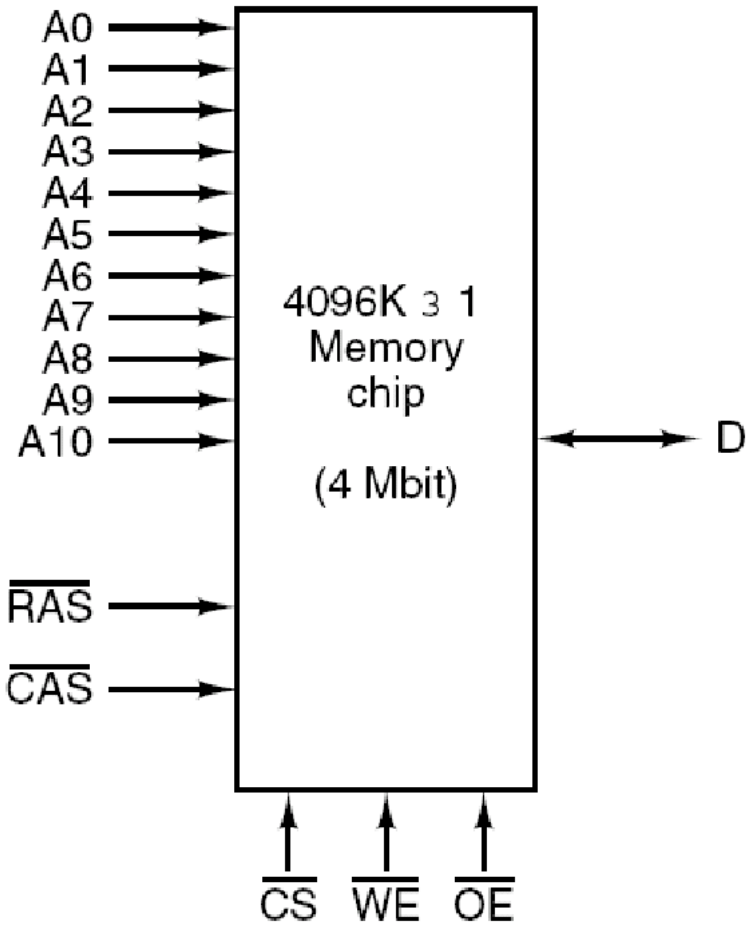
4-Mbits minnebrikke





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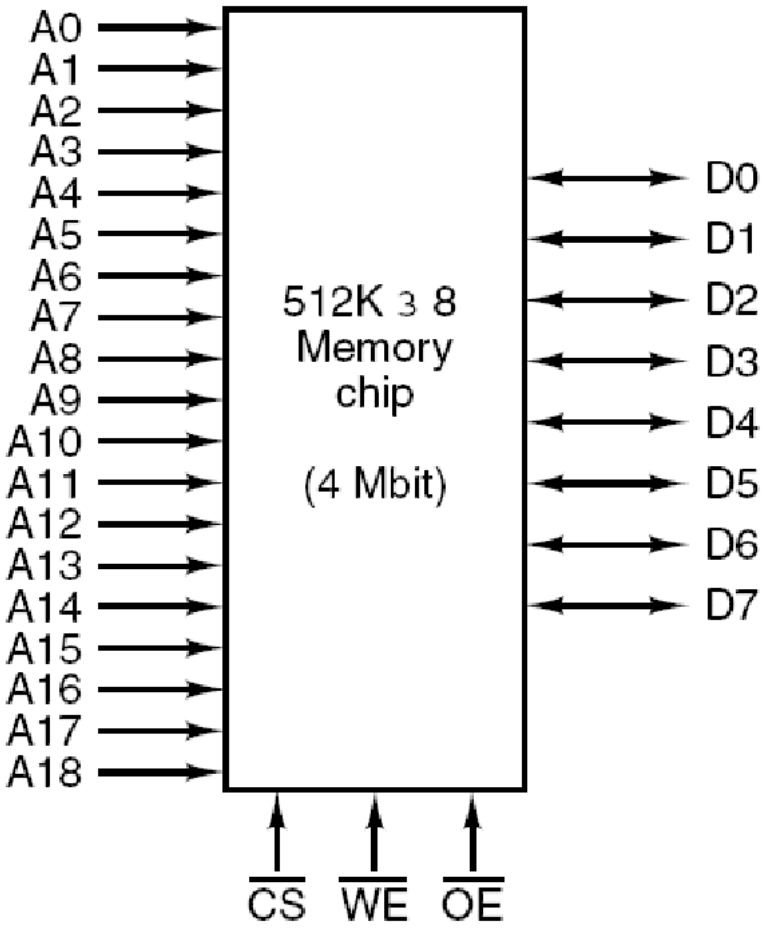
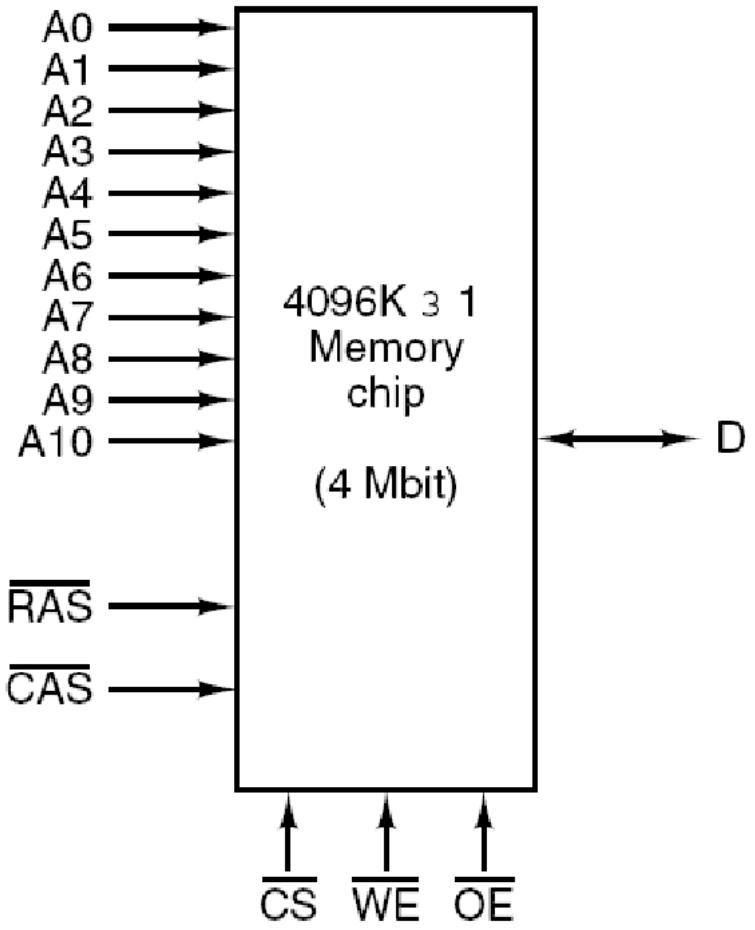
Random Access Memory (RAM)

- Data kan aksesseres i tilfeldig rekkefølge
  - Direct Access Memory – harddisker
  - Serial Access Memory - bånd
- Krever strøm for å bevare innhold
- Statisk RAM
  - Matrise med D-flip-flop (= det vi har sett til nå)
  - 6 transistorer pr. bit
  - Dyrt, stort og raskt
- Dynamisk RAM
  - 1 transistor og 1 kondensator pr. bit
  - Billig, lite og ”tregt”
  - Krever oppfrisking

4-Mbits minnebrikke





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